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1 Bit Logic Instructions

1.1 Overview of Bit Logic Instructions Description

Bit logic instructions work with two digits, 1 and 0.

These two digits form the base of a number system called the binary system.

The two digits 1 and 0 are called binary digits or bits. In the world of contacts and coils, a 1 indicates activated or energized, and a 0 indicates not activated or not energized.

The bit logic instructions interpret signal states of 1 and 0 and combine them according to Boolean logic.

These combinations produce a result of 1 or 0 that is called the "result of logic operation" (RLO).

The logic operations that are triggered by the bit logic instructions perform a variety of functions.

There are bit logic instructions to perform the following functions:

- ---| |--- Normally Open Contact (Address)
- ---| / |--- Normally Closed Contact (Address)
- ---(SAVE) Save RLO into BR Memory
- XOR Bit Exclusive OR
- ---() Output Coil
- ---(#)--- Midline Output

- ---|NOT|--- Invert Power Flow

The following instructions react to an RLO of 1:

- ---(S) Set Coil
- ---(R) Reset Coil
- SR Set-Reset Flip Flop
- RS Reset-Set Flip Flop

Other instructions react to a positive or negative edge transition to perform the following functions:

- ---(N)--- Negative RLO Edge Detection
- ---(P)--- Positive RLO Edge Detection
- NEG Address Negative Edge Detection
- POS Address Positive Edge Detection
- Immediate Read
- Immediate Write

1.2 ---| |--- Normally Open Contact (Address)

Symbol

<address>

---| |---

Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, L, D, T, C	Checked bit

Description

---| |--- (Normally Open Contact) is closed when the bit value stored at the specified <address> is equal to "1".

When the contact is closed, ladder rail power flows across the contact and the result of logic operation (RLO) = "1".

Otherwise, if the signal state at the specified <address> is "0", the contact is open.

When the contact is open, power does not flow across the contact and the result of logic operation (RLO) = "0".

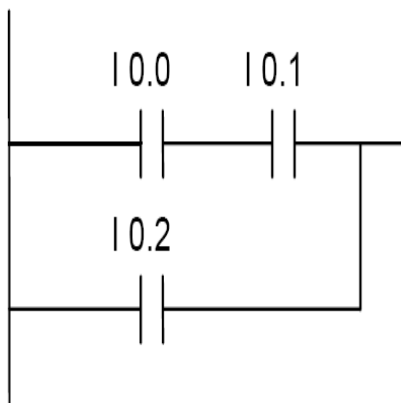
When used in series, ---| |--- is linked to the RLO bit by AND logic.

When used in parallel, it is linked to the RLO by OR logic.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



Power flows if one of the following conditions exists:

The signal state is "1" at inputs I0.0 and I0.1

Or the signal state is "1" at input I0.2

1.3 ---| / |--- Normally Closed Contact (Address)

Symbol

<address>

---| / |---

Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, L, D, T, C	Checked bit

Description

---| / |--- (Normally Closed Contact) is closed when the bit value stored at the specified <address> is equal to "0". When the contact is closed, ladder rail power flows across the contact and the result of logic operation (RLO) = "1". Otherwise, if the signal state at the specified <address> is "1", the contact is opened.

When the contact is opened, power does not flow across the contact and the result of logic operation (RLO) = "0".

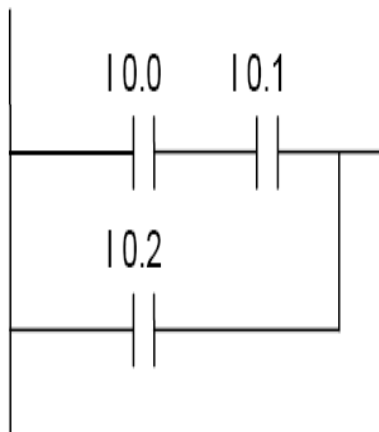
When used in series, ---| / |--- is linked to the RLO bit by AND logic.

When used in parallel, it is linked to the RLO by OR logic.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



Power flows if one of the following conditions exists:

The signal state is "1" at inputs I0.0 and I0.1

Or the signal state is "1" at input I0.2

1.3 ---| / |-- Normally Closed Contact (Address)

Symbol

<address>

---| / |--

Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, L, D, T, C	Checked bit

Description

---| / |-- (Normally Closed Contact) is closed when the bit value stored at the specified <address> is equal to "0".

When the contact is closed, ladder rail power flows across the contact and the result of logic operation (RLO) = "1".

Otherwise, if the signal state at the specified <address> is "1", the contact is opened.

When the contact is opened, power does not flow across the contact and the result of logic operation (RLO) = "0".

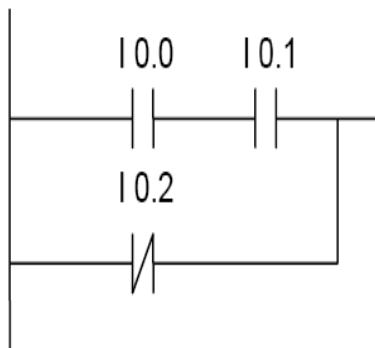
When used in series, ---| / |-- is linked to the RLO bit by AND logic.

When used in parallel, it is linked to the RLO by OR logic.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



Power flows if one of the following conditions exists:

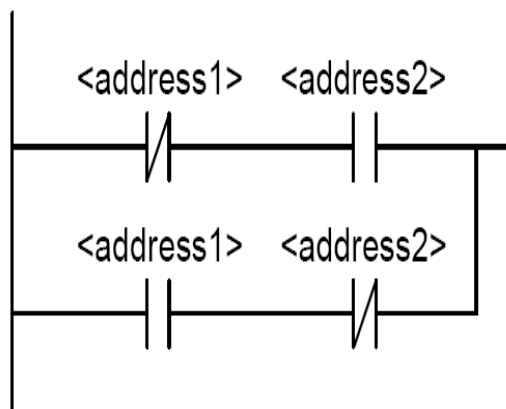
The signal state is "1" at inputs I0.0 and I0.1

Or the signal state is "1" at input I0.2

1.4 XOR Bit Exclusive OR

For the XOR function, a network of normally open and normally closed contacts must be created as shown below.

Symbols

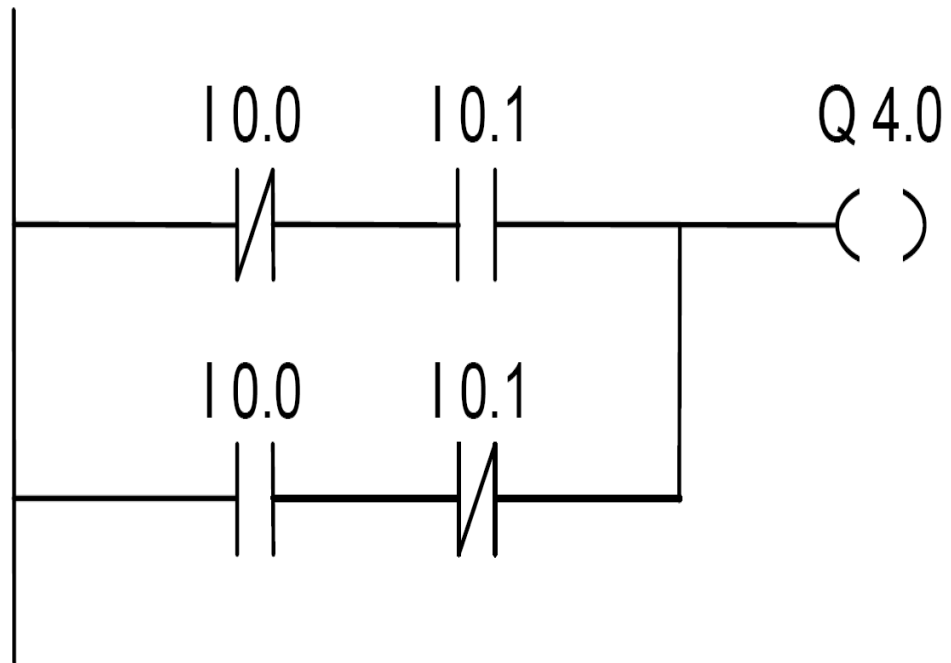


Parameter	Data Type	Memory Area	Description
<address1>	BOOL	I, Q, M, L, D, T, C	Scanned bit
<address2>	BOOL	I, Q, M, L, D, T, C	Scanned bit

Description

XOR (Bit Exclusive OR) creates an RLO of "1" if the signal state of the two specified bits is different.

Example



The output Q4.0 is "1" if (I0.0 = "0" AND I0.1 = "1") OR (I0.0 = "1" AND I0.1 = "0") .

1.5 --|NOT|-- Invert Power Flow

Symbol

---|NOT|---

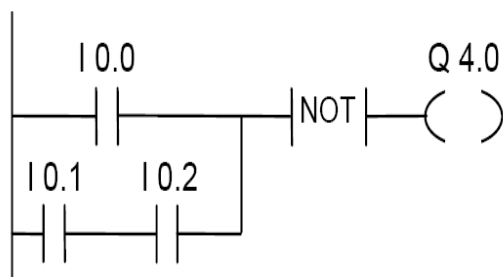
Description

---|NOT|--- (Invert Power Flow) negates the RLO bit.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	-	1	X	-

Example



The signal state of output Q4.0 is "0" if one of the following conditions exists:

The signal state is "1" at input I0.0

Or the signal state is "1" at inputs I0.1 and I0.2.

1.6 ---() Output Coil

Symbol

<address>

---()

Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, L, D	Assigned bit

Description

---() (Output Coil) works like a coil in a relay logic diagram.

If there is power flow to the coil (RLO = 1), the bit at location <address> is set to "1".

If there is no power flow to the coil (RLO = 0), the bit at location <address> is set to "0".

An output coil can only be placed at the right end of a ladder rung. Multiple output elements (max. 16) are possible (see example).

A negated output can be created by using the ---|NOT|--- (invert power flow) element.

MCR (Master Control Relay) dependency

MCR dependency is activated only if an output coil is placed inside an active MCR zone.

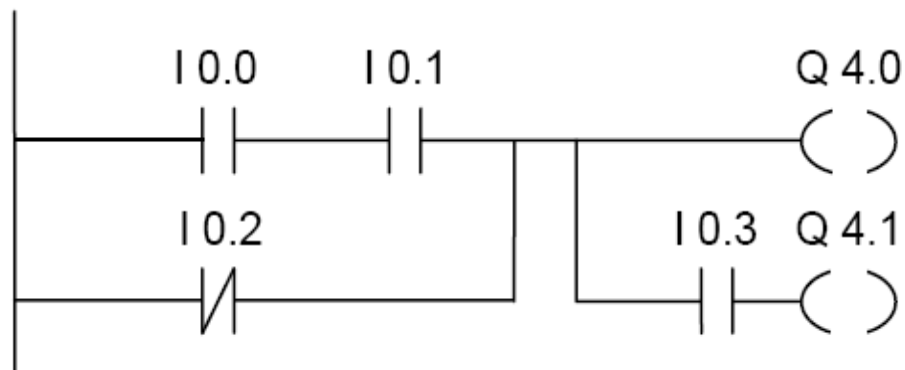
Within an activated MCR zone, if the MCR is on and there is power flow to an output coil; the addressed bit is set to the current status of power flow.

If the MCR is off, a logic "0" is written to the specified address regardless of power flow status.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	X	-	0

Example



The signal state of output Q4.0 is "1" if one of the following conditions exists:

The signal state is "1" at inputs I0.0 and I0.1 Or the signal state is "0" at input I0.2.

The signal state of output Q4.1 is "1" if one of the following conditions exists:

The signal state is "1" at inputs I0.0 and I0.1

Or the signal state is "0" at input I0.2 and "1" at input I0.3

If the example rungs are within an activated MCR zone:

When MCR is on, Q4.0 and Q4.1 are set according to power flow status as described above.

When MCR is off (=0), Q4.0 and Q4.1 are reset to 0 regardless of power flow.

1.7 ---(#)--- Midline Output

Symbol

<address>

---(#)---

Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, *L, D	Assigned bit

- An L area address can only be used if it is declared

TEMP in the variable

declaration table of a logic block (FC, FB, OB).

Description

---(#)--- (Midline Output) is an intermediate assigning element which saves the

RLO bit (power flow status) to a specified <address>.

The midline output element saves the logical result of the preceding branch elements.

In series with other contacts, ---(#)--- is inserted like a contact.

A ---(#)--- element may never be connected to the power rail or directly after a branch connection or at the end of a branch.

A negated ---(#)--- can be created by using the ---|NOT|--- (invert power flow) element.

MCR (Master Control Relay) dependency

MCR dependency is activated only if a midline output coil is placed inside an active MCR zone.

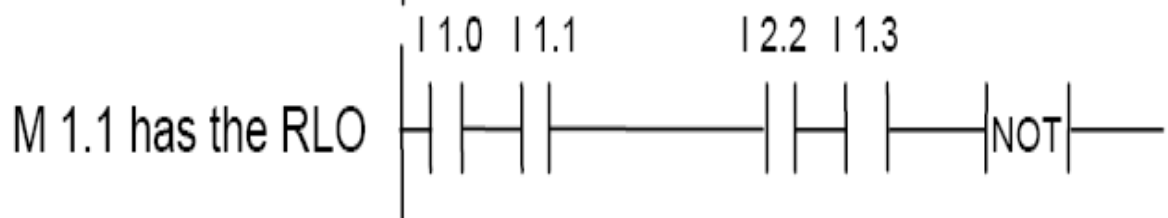
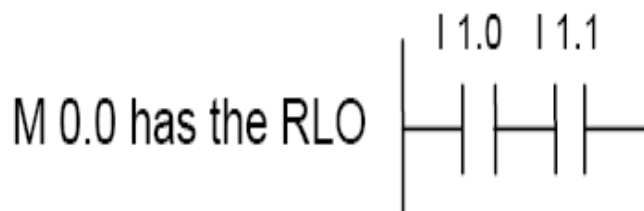
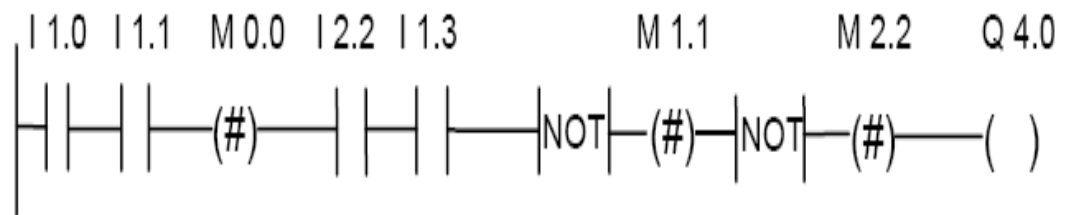
Within an activated MCR zone, if the MCR is on and there is power flow to a midline output coil; the addressed bit is set to the current status of powerflow.

If the MCR is off, a logic "0" is written to the specified address regardless of power flow status.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	X	-	1

Example



M 2.2 has the RLO of the entire bit logic combination

1.8 ---(R) Reset Coil

Symbol

<address>

---(R)

Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, L, D, T, C	Reset bit

Description

---(R) (Reset Coil) is executed only if the RLO of the preceding instructions is "1" (power flows to the coil). If power flows to the coil (RLO is "1"), the specified <address> of the element is reset to "0".

A RLO of "0" (no power flow to the coil) has no effect and the state of the element's specified address remains unchanged.

The <address> may also be a timer (T no.) whose timer value is reset to "0" or a counter (C no.) whose counter value is reset to "0".

MCR (Master Control Relay) dependency

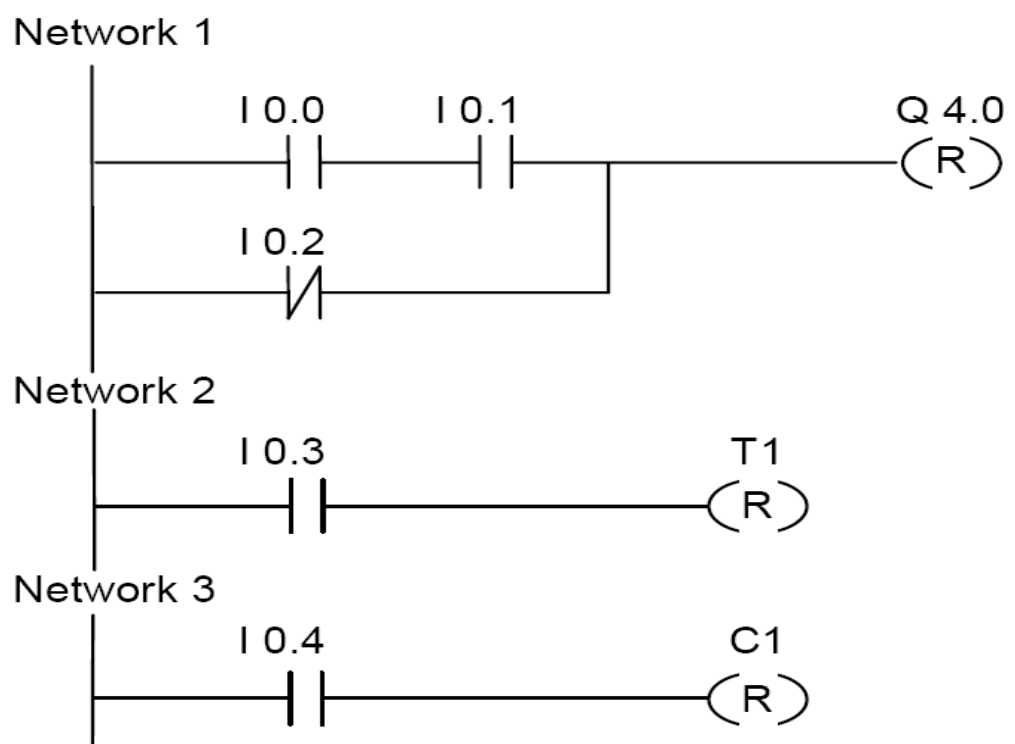
MCR dependency is activated only if a reset coil is placed inside an active MCR zone.

Within an activated MCR zone, if the MCR is on and there is power flow to a reset coil; the addressed bit is reset to the "0" state. If the MCR is off, the current state of the element's specified address remains unchanged regardless of power flow status.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	X	-	0

Example



The signal state of output Q4.0 is reset to "0" if one of the following conditions exists:

The signal state is "1" at inputs I0.0 and I0.1 Or the signal state is "0" at input I0.2.

If the RLO is "0", the signal state of output Q4.0 remains unchanged.

The signal state of timer T1 is only reset if:

the signal state is "1" at input I0.3.

The signal state of counter C1 is only reset if:

the signal state is "1" at input I0.4.

If the example rungs are within an activated MCR zone:

When MCR is on, Q4.0, T1, and C1 are reset as described above.

When MCR is off, Q4.0, T1, and C1 are left unchanged regardless of RLO state (power flow status).

1.9 ---(S) Set Coil

Symbol

<address>

---(S)

Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, L, D	Set bit

Description

---(S) (Set Coil) is executed only if the RLO of the preceding instructions is "1" (power flows to the coil). If the RLO is "1" the specified <address> of the element is set to "1".

An RLO = 0 has no effect and the current state of the element's specified address remains unchanged.

MCR (Master Control Relay)

dependency MCR dependency is activated only if a set coil is placed inside an active MCR zone.

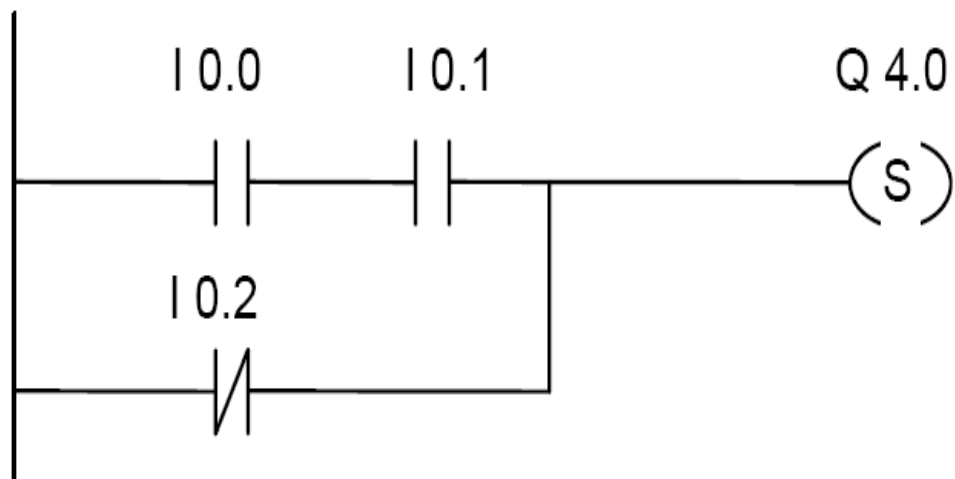
Within an activated MCR zone, if the MCR is on and there is power flow to a set coil; the addressed bit is set to the "1" state.

If the MCR is off, the current state of the element's specified address remains unchanged regardless of power flow status.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	X	-	0

Example



The signal state of output Q4.0 is "1" if one of the following conditions exists:

The signal state is "1" at inputs I0.0 and I0.1 Or the signal state is "0" at input I0.2.

If the RLO is "0", the signal state of output Q4.0 remains unchanged.

If the example rungs are within an activated MCR

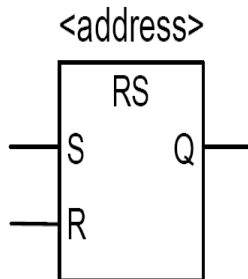
zone:

When MCR is on, Q4.0 is set as described above.

When MCR is off, Q4.0 is left unchanged regardless of RLO state (power flow status).

1.10 RS Reset-Set Flip Flop

Symbol



Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, L, D	Set or reset bit
S	BOOL	I, Q, M, L, D	Enabled reset instruction
R	BOOL	I, Q, M, L, D	Enabled reset instruction
Q	BOOL	I, Q, M, L, D	Signal state of <address>

Description

RS (Reset-Set Flip Flop) is reset if the signal state is "1" at the R input, and "0" at the S input.

Otherwise, if the signal state is "0" at the R input and "1" at the S input, the flip flop is set.

If the RLO is "1" at both inputs, the order is of primary importance.

The RS flip flop executes first the reset instruction then the set

instruction at the specified <address>, so that this address remains set for the remainder of program scanning.

The S (Set) and R (Reset) instructions are executed only when the RLO is "1".

RLO "0" has no effect on these instructions and the address specified in the instruction remains unchanged.

MCR (Master Control Relay) dependency

MCR dependency is activated only if a RS flip flop is placed inside an active MCR zone.

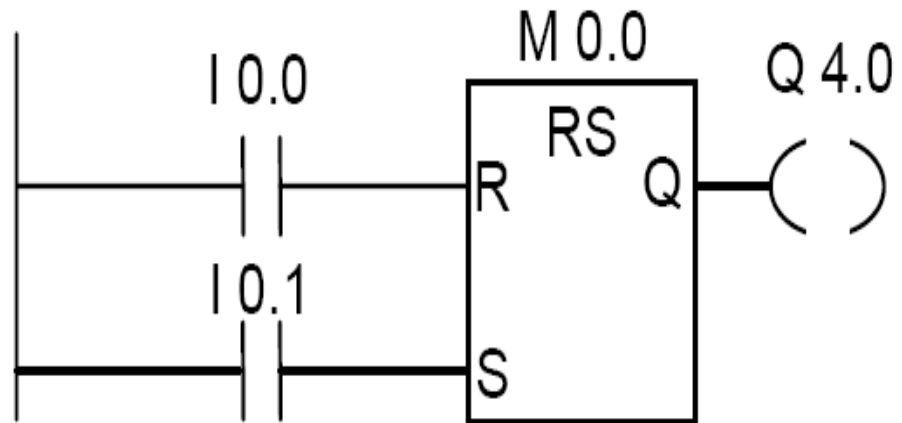
Within an activated MCR zone, if the MCR is on, the addressed bit is reset to "0" or set to "1" as described above.

If the MCR is off, the current state of the specified address remains unchanged regardless of input states.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



If the signal state is "1" at input I0.0 and "0" at I0.1, memory bit M0.0 is set and output Q4.0 is "0".

Otherwise, if the signal state at input I0.0 is "0" and at I0.1 is "1", memory bit M0.0 is reset and output Q4.0 is "1".

If both signal states are "0", nothing is changed.

If both signal states are "1", the set instruction dominates because of the order; M0.0 is set and Q4.0 is "1".

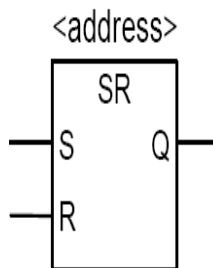
If the example is within an activated MCR zone:

When MCR is on, Q4.0 is reset or set as described above.

When MCR is off, Q4.0 is left unchanged regardless of input states.

1.11 SR Set-Reset Flip Flop

Symbol



Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, L, D	Set or reset bit
S	BOOL	I, Q, M, L, D	Enable set instruction
R	BOOL	I, Q, M, L, D	Enable reset instruction
Q	BOOL	I, Q, M, L, D	Signal state of <address>

Description

SR (Set-Reset Flip Flop) is set if the signal state is "1" at the S input, and "0" at the R input.

Otherwise, if the signal state is "0" at the S input and "1" at the R input, the flip flop is reset.

If the RLO is "1" at both inputs, the order is of primary importance.

The SR flip flop executes first the set instruction then the reset

Instruction at the specified <address>, so that this address remains reset for the remainder of program scanning.

The S (Set) and R (Reset) instructions are executed only when the RLO is "1".

RLO "0" has no effect on these instructions and the address specified in the instruction remains unchanged.

MCR (Master Control Relay) dependency

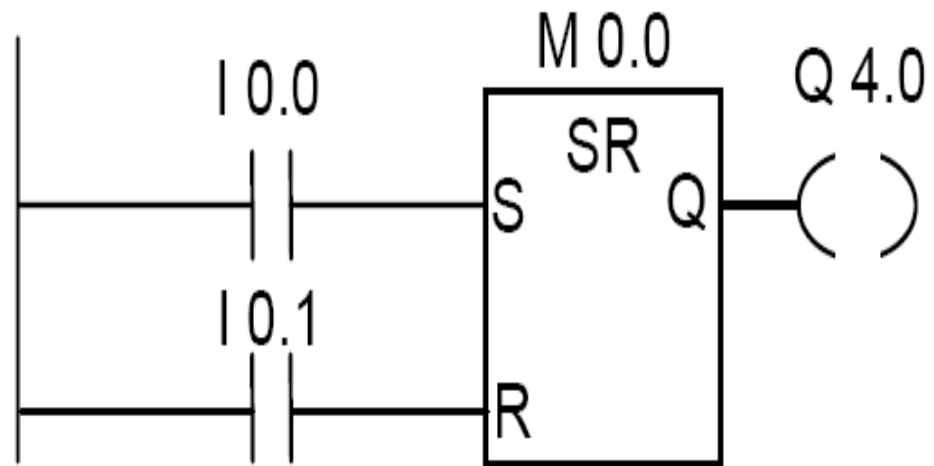
MCR dependency is activated only if a SR flip flop is placed inside an active MCR zone.

Within an activated MCR zone, if the MCR is on ; the addressed bit is set to "1" or reset to "0" as described above. If the MCR is off, the current state of the specified address remains unchanged regardless of input states.

Status word

	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



If the signal state is "1" at input I0.0 and "0" at I0.1, memory bit M0.0 is set and output Q4.0 is "1".

Otherwise, if the signal state at input I0.0 is "0" and at I0.1 is "1", memory bit M0.0 is reset and output Q4.0 is "0". If both signal states are "0", nothing is changed.

If both signal states are "1", the reset instruction dominates because of the order; M0.0 is reset and Q4.0 is "0".

If the example is within an activated MCR zone:

When MCR is on, Q4.0 is set or reset as described above.

When MCR is off, Q4.0 is left unchanged regardless of input states.

1.12 ---(N)--- Negative RLO Edge Detection

Symbol

<address>

---(N)

Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, L, D	Edge memory bit, storing the previous signal state of RLO

Description

---(N)--- (Negative RLO Edge Detection) detects a signal change in the address from "1" to "0" and displays it as RLO = "1" after the instruction. The current signal state in the RLO is compared with the signal state of the address, the edge memory bit.

If the signal state of the address is "1" and the RLO was "0" before the instruction,

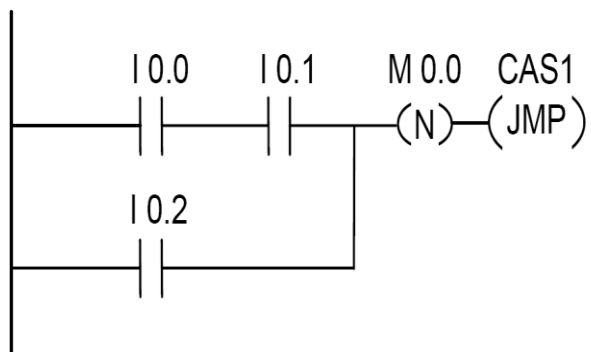
the RLO will be "1" (pulse) after this instruction, and "0" in all other cases.

The RLO prior to the instruction is stored in the address.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	x	x	1

Example



The edge memory bit M0.0 saves the old RLO state. When there is a signal change at the RLO from "1" to "0", the program jumps to label CAS1.

1.13 ---(P)--- Positive RLO Edge Detection

Symbol

<address>

---(P)---

Parameter	Data Type	Memory Area	Description
<address>	BOOL	I, Q, M, L, D	Edge memory bit, storing the previous signal state of RLO

Description

---(P)--- (Positive RLO Edge Detection) detects a signal change in the address from "0" to "1" and displays it as RLO = "1" after the instruction. The current signal state in the RLO is compared with the signal state of the address, the edge memory bit.

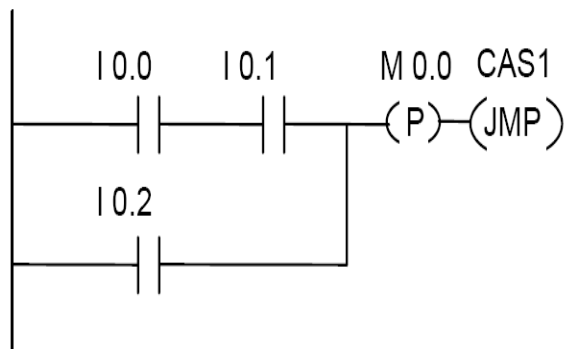
If the signal state of the address is "0" and the RLO was "1" before the instruction, the RLO will be "1" (pulse) after this instruction, and "0" in all other cases.

The RLO prior to the instruction is stored in the address.

Status word

	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	X	X	1

Example



The edge memory bit M0.0 saves the old RLO state. When there is a signal change at the RLO from "0" to "1", the program jumps to label CAS1.

1.14 ---(SAVE) Save RLO into BR Memory

Symbol

---(SAVE)

Description

---(SAVE) (Save RLO into BR Memory) saves the RLO to the BR bit of the status word.

The first check bit /FC is not reset. For this reason, the status of the BR bit is included in the AND logic operation in the next network.

For the instruction "SAVE" (LAD, FBD, STL), the following applies and not the

recommended use specified in the manual and

online help:

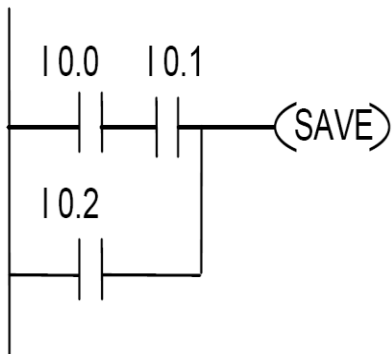
We do not recommend that you use SAVE and then check the BR bit in the same block or in subordinate blocks, because the BR bit can be modified by many instructions occurring inbetween.

It is advisable to use the SAVE instruction before exiting a block, since the ENO output (= BR bit) is then set to the value of the RLO bit and you can then check for errors in the block.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	-	-	-	-	-	-	-	-

Example

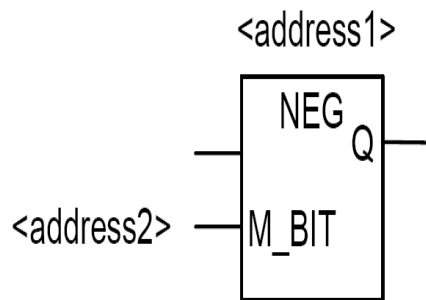


The status of the rung (=RLO) is saved to the BR bit.

BR Binary Result Bit (Status Word, Bit 8)

1.15 NEG Address Negative Edge Detection

Symbol



Parameter	Data Type	Memory Area	Description
<address1>	BOOL	I, Q, M, L, D	Scanned signal
<address2>	BOOL	I, Q, M, L, D	M_BIT edge memory bit, storing the previous signal state of <address1>
Q	BOOL	I, Q, M, L, D	One shot output

Description

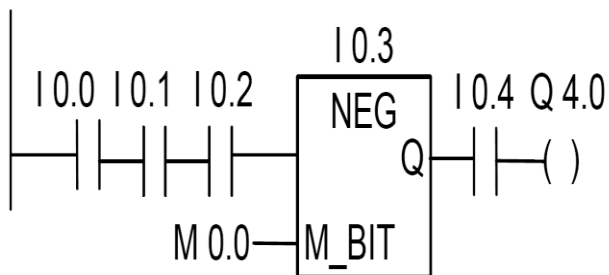
NEG (Address Negative Edge Detection) compares the signal state of <address1> with the signal state from the previous scan, which is stored in <address2> .

If the current RLO state is "1" and the previous state was "0" (detection of rising edge), the RLO bit will be "1" after this instruction.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	x	1	x	1

Example

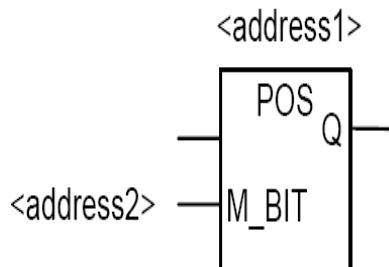


The signal state at output Q4.0 is "1" if the following conditions exist:

- The signal state is "1" at inputs I0.0 and I0.1 and I0.2
- And there is a negative edge at input I0.3
- And the signal state is "1" at input I0.4

1.16 POS Address Positive Edge Detection

Symbol



Parameter	Data Type	Memory Area	Description
<address1>	BOOL	I, Q, M, L, D	Scanned signal
<address2>	BOOL	I, Q, M, L, D	M_BIT edge memory bit, storing the previous signal state of <address1>
Q	BOOL	I, Q, M, L, D	One shot output

Description

POS (Address Positive Edge Detection) compares the signal state of <address1> with the signal state from the previous scan, which is stored in <address2>.

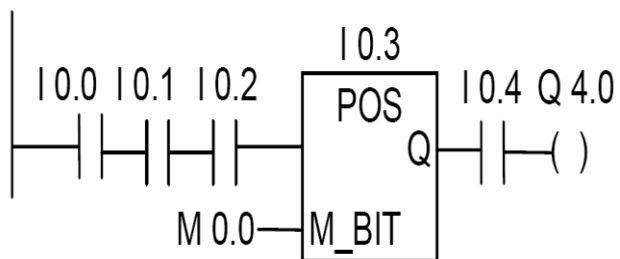
If the current RLO state is "1" and the previous state was "0"

(detection of rising edge), the RLO bit will be "1" after this instruction.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	x	1	x	1

Example



The signal state at output Q4.0 is "1" if the following conditions exist:

- The signal state is "1" at inputs I0.0 and I0.1 and I0.2
- And there is a positive edge at input I0.3
- And the signal state is "1" at input I0.4

1.17 Immediate Read

Description

For the Immediate Read function, a network of symbols must be created as shown in the example below.

For time-critical applications, the current state of a digital input may be read faster than the normal case of once per OB1 scan cycle. An Immediate Read gets the state of a digital input from an input module at the time the Immediate Read rung is scanned. Otherwise, you must wait for the end of the next OB1 scan cycle when the I memory area is updated with the P memory state.

To perform an immediate read of an input (or inputs) from an input module, use the peripheral input (PI) memory area instead of the input (I) memory area.

The peripheral input memory area can be read as a byte, a word, or a double word.

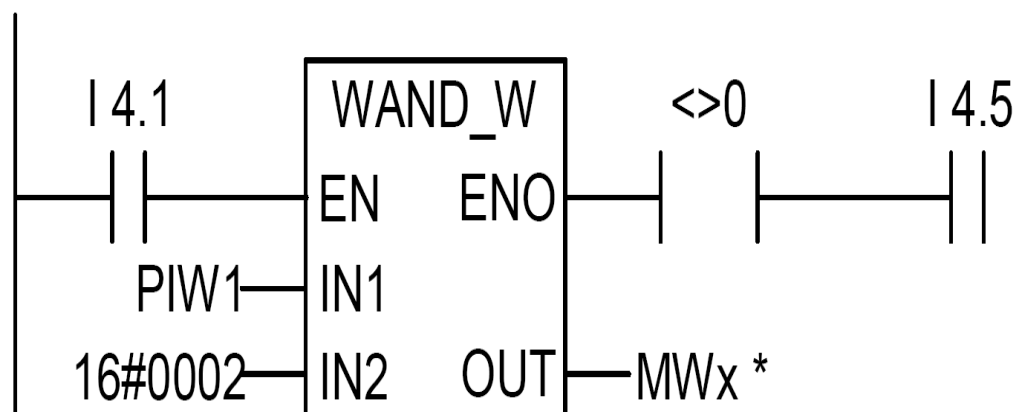
Therefore, a single digital input cannot be read via a contact (bit) element.

To conditionally pass voltage depending on the status of an immediate input:

1. A word of PI memory that contains the input data of concern is read by the CPU.
2. The word of PI memory is then ANDed with a constant that yields a non-zero result if the input bit is on ("1").
3. The accumulator is tested for non-zero condition.

Example

Ladder Network with Immediate Read of Peripheral



* MWx has to be specified in order to be able to store the network.

x may be any

permitted number

Description of WAND_W instruction:

PIW1	0000000000101010
W#16#0002	0000000000000010
Result	0000000000000010

In this example immediate input I1.1 is in series with I4.1 and I4.5.

The word PIW1 contains the immediate status of I1.1. PIW1 is ANDed with W#16#0002.

The result is not equal to zero if I1.1 (second bit) in PB1 is true ("1").

The contact A<>0 passes voltage if the result of the WAND_W instruction is not equal to zero.

1.18 Immediate Write

Description

For the Immediate Write function, a network of symbols must be created as shown in the example below.

For time-critical applications, the current state of a digital output may have to be sent to an output module faster than the normal case of once at the end of the OB1 scan cycle.

An Immediate Write writes to a digital output to a input module at the time the Immediate Write rung is scanned.

Otherwise, you must wait for the end of the next OB1 scan cycle when the Q memory area is updated with the P memory state.

To perform an immediate write of an output (or outputs) to an output module, use the peripheral output (PQ) memory area instead of the output (Q) memory area.

The peripheral output memory area can be read as a byte, a word, or a double word.

Therefore, a single digital output cannot be updated via a coil element.

To write the state of a digital output to an output module immediately, a byte, word, or double word of Q memory that contains the relevant bit is conditionally copied to the corresponding PQ memory (direct output module addresses).

Example

Ladder network equivalent of Immediate Write to peripheral digital output module 5, channel 1.

The bit states of the addressed output Q byte (QB5) are either modified or left unchanged.

Q5.1 is assigned the signal state of I0.1 in network 1. QB5 is copied to the corresponding direct peripheral output memory area (PQB5).

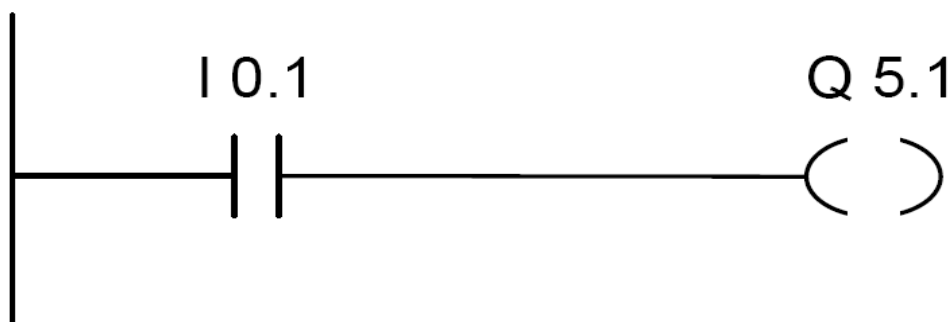
The word PIW1 contains the immediate status of I1.1.

PIW1 is ANDed with W#16#0002.

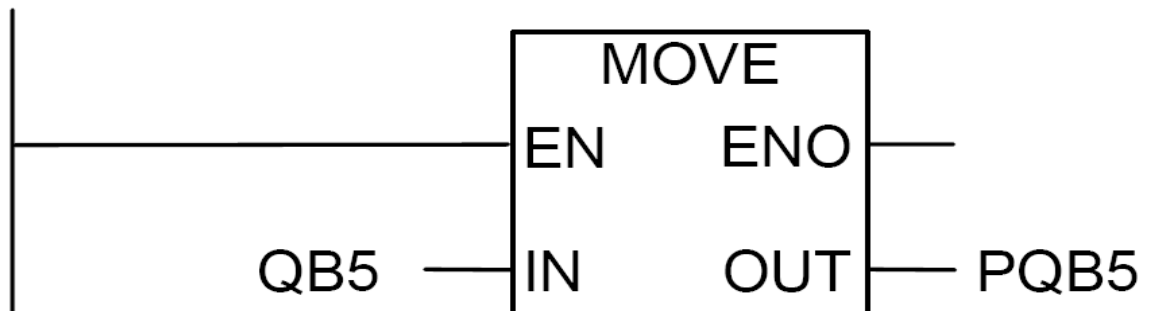
The result is not equal to zero if I1.1 (second bit) in PB1 is true ("1").

The contact A<>0 passes voltage if the result of the WAND_W instruction is not equal to zero.

Network 1



Network 2



In this example Q5.1 is the desired immediate output bit.

The byte PQB5 contains the immediate output status of the bit Q5.1.

The other 7 bits in PQB5 are also updated by the MOVE (copy) instruction .

2 Comparison Instructions

2.1 Overview of Comparison Instructions

Description

IN1 and IN2 are compared according to the type of comparison you choose:

== IN1 is equal to IN2

<> IN1 is not equal to IN2

> IN1 is greater than IN2

< IN1 is less than IN2

>= IN1 is greater than or equal to IN2

<= IN1 is less than or equal to IN2

If the comparison is true, the RLO of the function is "1".

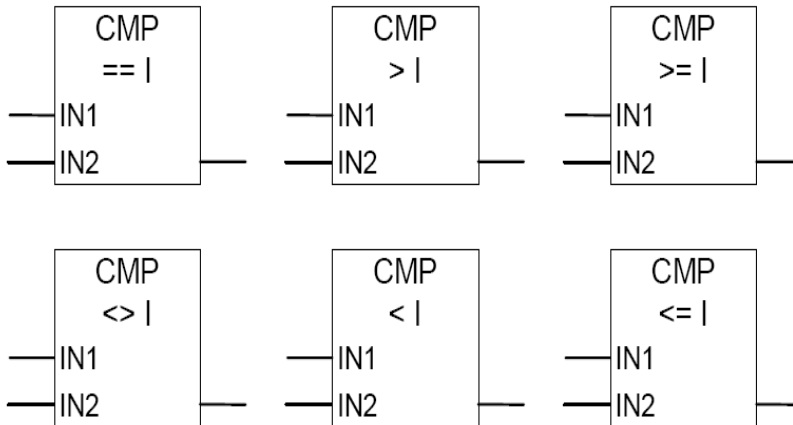
It is linked to the RLO of a rung network by AND if the compare element is used in series, or by OR if the box is used in parallel.

The following comparison instructions are available:

- CMP ? I Compare Integer
- CMP ? D Compare Double Integer
- CMP

2.2 CMP ? I Compare Integer

Symbols



Parameter	Data Type	Memory Area	Description
box input	BOOL	I, Q, M, L, D	Result of the previous logic operation
box output	BOOL	I, Q, M, L, D	Result of the comparison, is only processed further if the RLO at the box input = 1
IN1	INT	I, Q, M, L, D or constant	First value to compare
IN2	INT	I, Q, M, L, D or constant	Second value to compare

Description

CMP ? I (Compare Integer) can be used like a normal contact.

It can be located at any position where a normal contact could be placed. IN1 and IN2 are compared according to the type of comparison you choose.

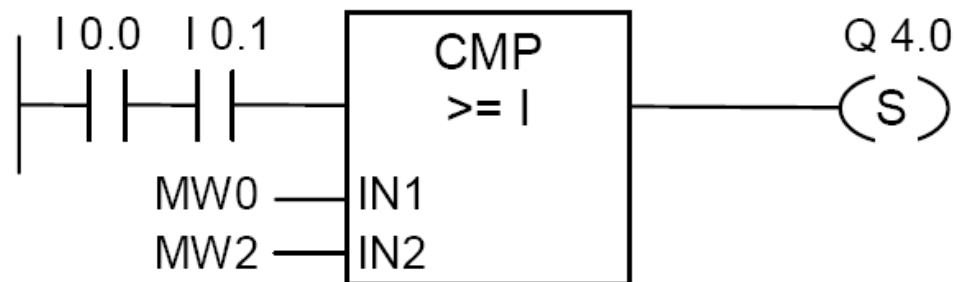
If the comparison is true, the RLO of the function is "1".

It is linked to the RLO of the whole rung by AND if the box is used in series, or by OR if the box is used in parallel.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	0	-	0	X	X	1

Example

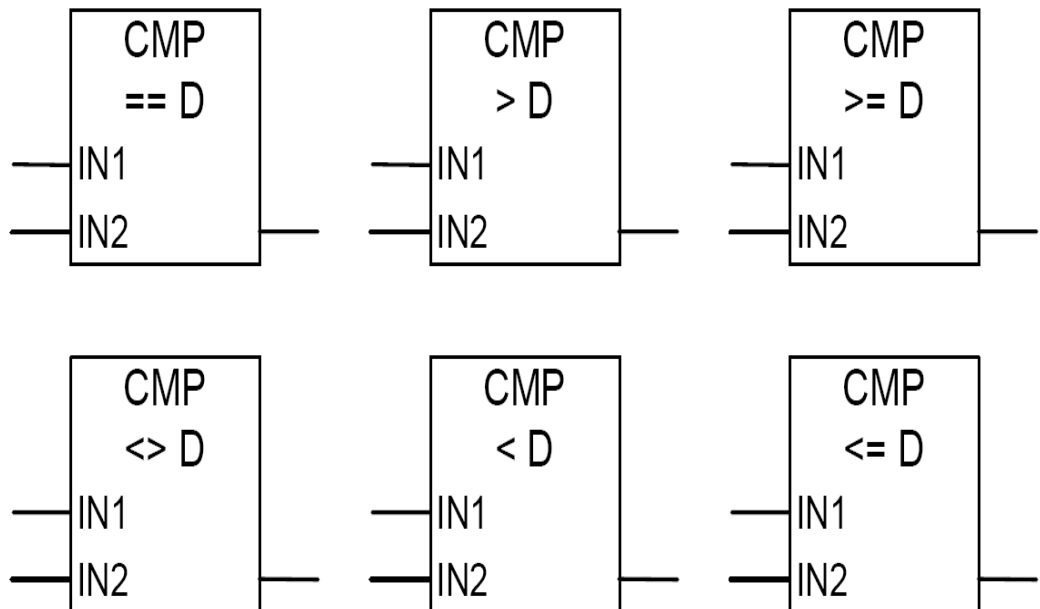


Output Q4.0 is set if the following conditions exist:

- There is a signal state of "1" at inputs I0.0 and at I0.1
- AND MW0 >= MW2

2.3 CMP ? D Compare Double Integer

Symbols



Parameter	Data Type	Memory Area	Description
box input	BOOL	I, Q, M, L, D	Result of the previous logic operation
box output	BOOL	I, Q, M, L, D	Result of the comparison, is only processed further if the RLO at the box input = 1
IN1	DINT	I, Q, M, L, D or constant	First value to compare
IN2	DINT	I, Q, M, L, D or constant	Second value to compare

Description

CMP ? D (Compare Double Integer) can be used like a normal contact. It can be located at any position where a normal contact could be placed.

IN1 and IN2 are compared according to the type of comparison you choose.

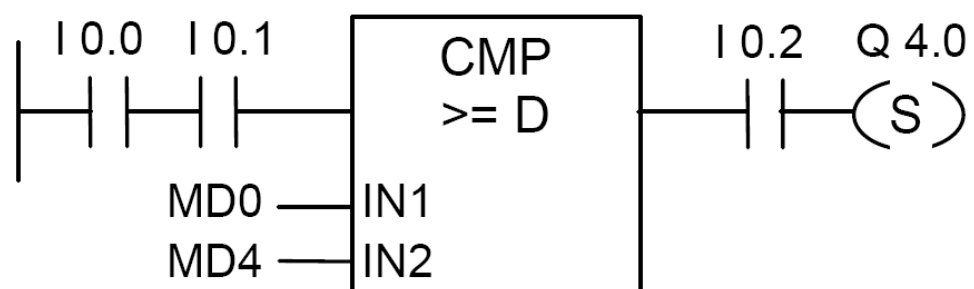
If the comparison is true, the RLO of the function is "1".

It is linked to the RLO of a rung network by AND if the compare element is used in series, or by OR if the box is used in parallel.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	0	-	0	X	X	1

Example

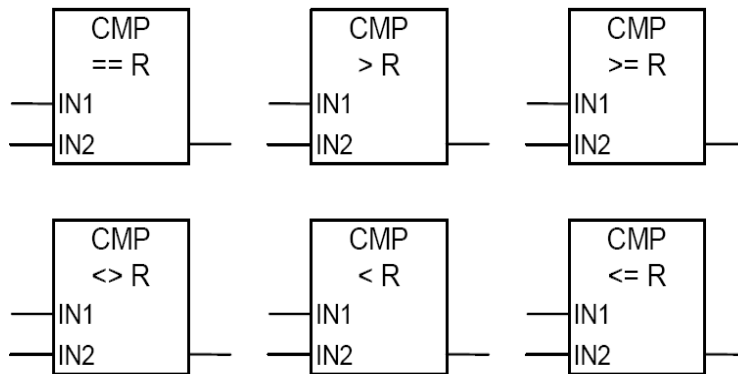


Output Q4.0 is set if the following conditions exist:

- There is a signal state of "1" at inputs I0.0 and at I0.1
- And MD0 >= MD4
- And there is a signal state of "1" at input I0.2

2.4 CMP ? R Compare Real

Symbols



Parameter	Data Type	Memory Area	Description
box input	BOOL	I, Q, M, L, D	Result of the previous logic operation
box output	BOOL	I, Q, M, L, D	Result of the comparison, is only processed further if the RLO at the box input = 1
IN1	REAL	I, Q, M, L, D or constant	First value to compare
IN2	REAL	I, Q, M, L, D or constant	Second value to compare

Description

CMP ? R (Compare Real) can be used like a normal contact. It can be located at any position where a normal contact could be placed.

IN1 and IN2 are compared according to the type of comparison you choose.

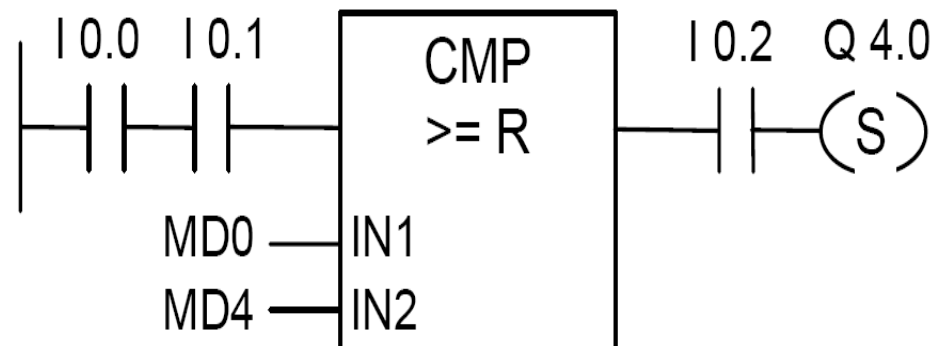
If the comparison is true, the RLO of the function is "1".

It is linked to the RLO of the whole rung by AND if the box is used in series, or by OR if the box is used in parallel.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



Output Q4.0 is set if the following conditions exist:

- There is a signal state of "1" at inputs I0.0 and at I0.1
- And MD0 >= MD4
- And there is a signal state of "1" at input I0.2

3 Conversion Instructions

3.1 Overview of Conversion Instructions

Description

The conversion instructions read the contents of the parameters IN and convert these or change the sign.

The result can be queried at the parameter OUT.

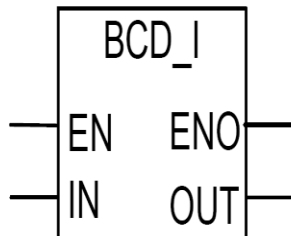
The following conversion instructions are available:

- BCD_I BCD to Integer
- I_BCD Integer to BCD
- BCD_DI BCD to Double Integer
- I_DINT Integer to Double Integer
- DI_BCD Double Integer to BCD
- DI_REAL Double Integer to Floating-Point
- INV_I Ones Complement Integer
- INV_DI Ones Complement Double Integer
- NEG_I Twos Complement Integer
- NEG_DI Twos Complement Double Integer
- NEG_R Negate Floating-Point Number

- ROUND Round to Double Integer
- TRUNC Truncate Double Integer Part
- CEIL Ceiling
- FLOOR Floor

3.2 BCD_I BCD to Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	WORD	I, Q, M, L, D	BCD number
OUT	INT	I, Q, M, L, D	Integer value of BCD number

Description

BCD_I (Convert BCD to Integer) reads the contents of the IN parameter as a threedigit, BCD coded number (+/- 999) and converts it to an integer value (16-bit) .

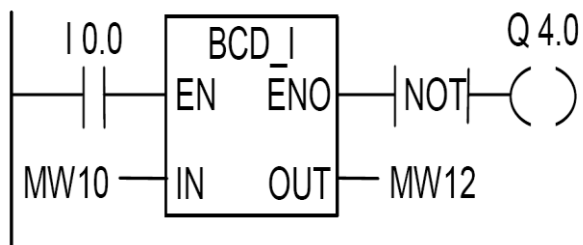
The integer result is output by the parameter OUT.

ENO always has the same signal state as EN .

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	-	-	-	-	0	1	1	1

Example



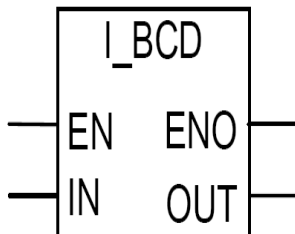
If input I0.0 is "1" , then the content of MW10 is read as a three-digit BCD coded number and converted to an integer.

The result is stored in MW12.

The output Q4.0 is "1" if the conversion is not executed (ENO = EN = 0).

3.3 I_BCD Integer to BCD

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	INT	I, Q, M, L, D	Integer number
OUT	WORD	I, Q, M, L, D	BCD value of integer number

Description

I_BCD (Convert Integer to BCD) reads the content of the IN parameter as an integer value (16-bit) and converts it to a three-digit BCD coded number (+/- 999).

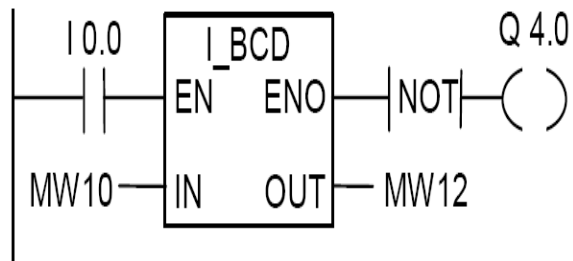
The result is output by the parameter OUT.

If an overflow occurred, ENO will be "0".

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	-	-	x	x	0	x	x	1

Example



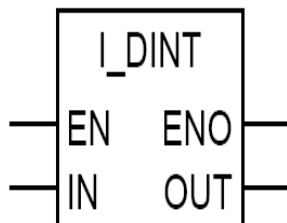
If I0.0 is "1", then the content of MW10 is read as an integer and converted to a three-digit BCD coded number.

The result is stored in MW12.

The output Q4.0 is "1" if there was an overflow, or the instruction was not executed (I0.0 = 0).

3.4 I_DINT Integer to Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	INT	I, Q, M, L, D	Integer value to convert
OUT	DINT	I, Q, M, L, D	Double integer result

Description

I_DINT (Convert Integer to Double Integer) reads the content of the IN parameter as an integer (16-bit) and converts it to a double integer (32-bit).

The result is output by the parameter OUT.

ENO always has the same signal state as EN.

If I0.0 is "1", then the content of MW10 is read as an integer and converted to a double integer.

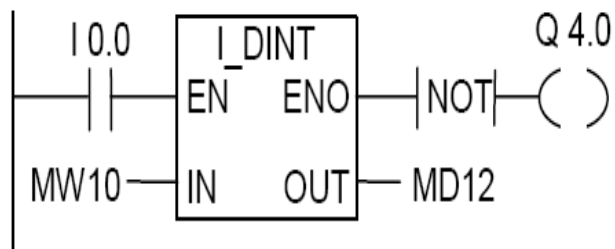
The result is stored in MD12.

The output Q4.0 is "1" if the conversion is not executed (ENO = EN = 0).

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	-	-	-	-	0	1	1	1

Example



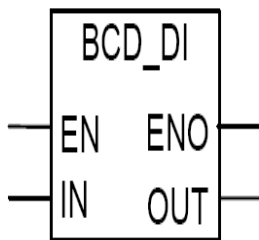
If I0.0 is "1", then the content of MW10 is read as an integer and converted to a double integer.

The result is stored in MD12.

The output Q4.0 is "1" if the conversion is not executed (ENO = EN = 0).

3.5 BCD_DI BCD to Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	DWORD	I, Q, M, L, D	BCD number
OUT	DINT	I, Q, M, L, D	Double integer value of BCD number

Description

BCD_DI (Convert BCD to Double Integer) reads the content of the IN parameter as a seven-digit, BCD coded number (+/- 9999999) and converts it to a double integer value (32-bit).

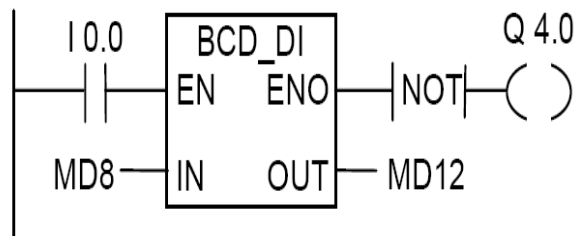
The double integer result is output by the parameter OUT.

ENO always has the same signal state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	-	-	-	-	0	1	1	1

Example



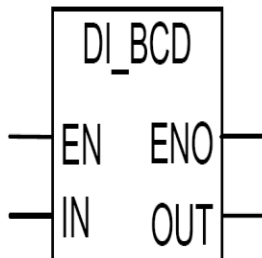
If I0.0 is "1", then the content of MD8 is read as a seven-digit BCD coded number and converted to a double integer.

The result is stored in MD12.

The output Q4.0 is "1" if the conversion is not executed (ENO = EN = 0).

3.6 DI_BCD Double Integer to BCD

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	DINT	I, Q, M, L, D	Double integer number
OUT	DWORD	I, Q, M, L, D	BCD value of a double integer number

Description

DI_BCD (Convert Double Integer to BCD) reads the content of the IN parameter as a double integer (32-bit) and converts it to a seven-digit BCD coded number (+/- 9999999).

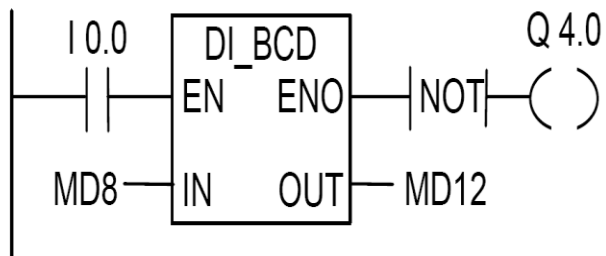
The result is output by the parameter OUT.

If an overflow occurred, ENO will be "0".

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	-	-	X	X	0	X	X	1

Example



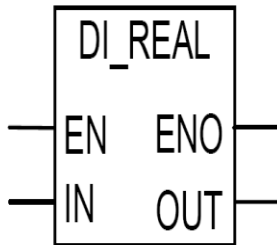
If I0.0 is "1", then the content of MD8 is read as a double integer and converted to a seven-digit BCD number.

The result is stored in MD12.

The output Q4.0 is "1" if an overflow occurred, or the instruction was not executed (I0.0 = 0).

3.7 DI_REAL Double Integer to Floating-Point

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	DINT	I, Q, M, L, D	Double integer value to convert
OUT	REAL	I, Q, M, L, D	Floating-point number result

Description

DI_REAL (Convert Double Integer to Floating-Point) reads the content of the IN parameter as a double integer and converts it to a floating-point number.

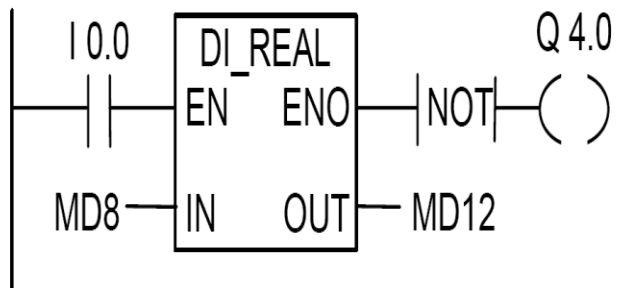
The result is output by the parameter OUT.

ENO always has the same signal state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	-	-	-	-	0	1	1	1

Example

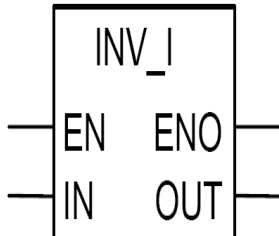


If I0.0 is "1", then the content of MD8 is read as a double integer and converted to a floating-point number.

The result is stored in MD12. The output Q4.0 is "1" if the conversion is not executed (ENO = EN = 0).

3.8 INV_I Ones Complement Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	INT	I, Q, M, L, D	Integer input value
OUT	INT	I, Q, M, L, D	Ones complement of the integer IN

Description

INV_I (Ones Complement Integer) reads the content of the IN parameter and performs a Boolean XOR function with the hexadecimal mask W#16#FFFF.

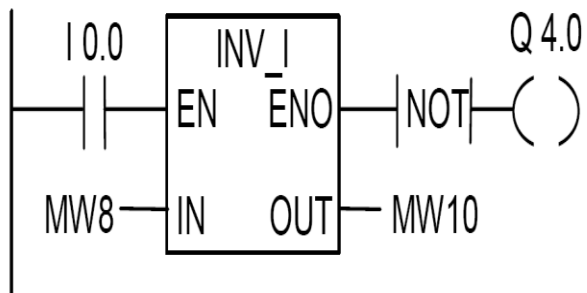
This instruction changes every bit to its opposite state.

ENO always has the same signal state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	-	-	-	-	0	1	1	1

Example



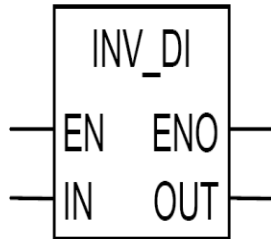
If I0.0 is "1", then every bit of MW8 is reversed, for example:

MW8 = 01000001 10000001 results in MW10 = 10111110 01111110.

The output Q4.0 is "1" if the conversion is not executed (ENO = EN = 0).

3.9 INV_DI Ones Complement Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	DINT	I, Q, M, L, D	Double integer input value
OUT	DINT	I, Q, M, L, D	Ones complement of the double integer IN

Description

INV_DI (Ones Complement Double Integer) reads the content of the IN parameter and performs a Boolean XOR function with the hexadecimal mask W#16#FFFF FFFF .

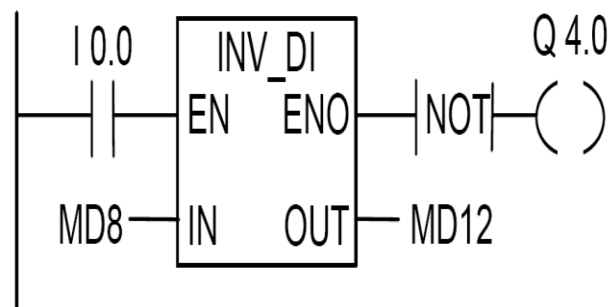
This instruction changes every bit to its opposite state.

ENO always has the same signal state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	-	-	-	-	0	1	1	1

Example



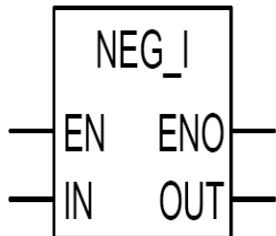
If I0.0 is "1", then every bit of MD8 is reversed, for example:

MD8 = F0FF FFF0 results in MD12 = 0F00 000F.

The output Q4.0 is "1" if the conversion is not executed (ENO = EN = 0).

3.10 NEG_I Twos Complement Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	INT	I, Q, M, L, D	Integer input value
OUT	INT	I, Q, M, L, D	Twos complement of integer IN

Description

NEG_I (Twos Complement Integer) reads the content of the IN parameter and performs a twos complement instruction. The twos complement instruction is equivalent to multiplication by (-1) and changes the sign (for example: from a positive to a negative value).

ENO always has the same signal state as EN with the following exception:

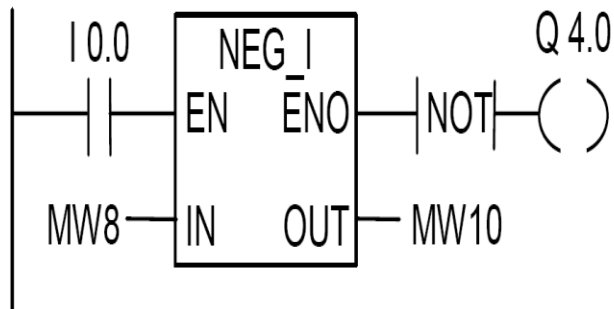
if the signal state of EN = 1 and

an overflow occurs, the signalstate of ENO = 0.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	X	0	X	X	1

Example



If I0.0 is "1", then the value of MW8 with the opposite sign is output by the OUT parameter to MW10.

MW8 = + 10 results in MW10 = - 10.

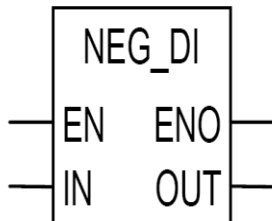
The output Q4.0 is "1" if the conversion is not executed (ENO = EN = 0).

If the signal state of EN = 1

and an overflow occurs, the signal state of ENO = 0.

3.11 NEG_DI Twos Complement Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	DINT	I, Q, M, L, D	Double integer input value
OUT	DINT	I, Q, M, L, D	Twos complement of IN value

Description

NEG_DI (Twos Complement Double Integer) reads the content of the IN parameter and performs a twos complement instruction.

The twos complement instruction is equivalent to multiplication by (-1) and changes the sign (for example:

from a positive to a negative value).

ENO always has the same signal state as EN with the following exception:

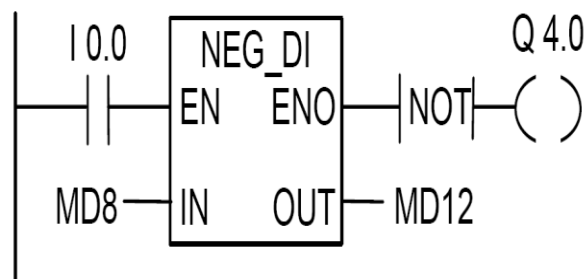
if the signal state of EN = 1 and an overflow occurs, the signal

state of ENO = 0.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	X	0	X	X	1

Example



If I0.0 is "1", then the value of MD8 with the opposite sign is output by the OUT parameter to MD12.

MD8 = + 1000 results in MD12 = - 1000.

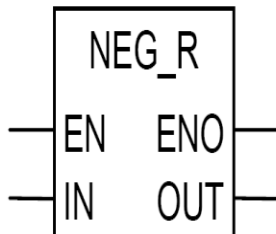
The output Q4.0 is "1" if the conversion is not executed (ENO = EN = 0).

If the signal state of EN = 1 and

an overflow occurs, the signal state of ENO = 0.

3.12 NEG_R Negate Floating-Point Number

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D	Floating-point number input value
OUT	REAL	I, Q, M, L, D	Floating-point number IN with negative sign

Description

NEG_R (Negate Floating-Point) reads the contents of the IN parameter and changes the sign.

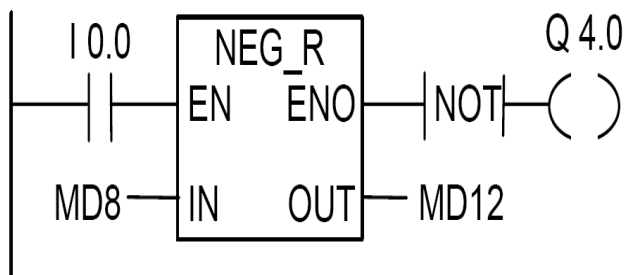
The instruction is equivalent to multiplication by (-1) and changes the sign (for example: from a positive to a negative value).

ENO always has the same signal state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	-	-	-	-	0	x	x	1

Example



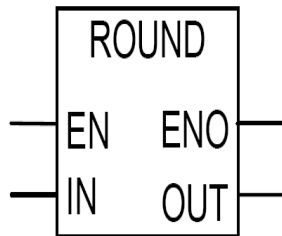
If I0.0 is "1", then the value of MD8 with the opposite sign is output by the OUT parameter to MD12.

MD8 = + 6.234 results in MD12 = - 6.234.

The output Q4.0 is "1" if the conversion is not executed (ENO = EN = 0).

3.13 ROUND Round to Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D	Value to round
OUT	DINT	I, Q, M, L, D	IN rounded to nearest whole number

Description

ROUND (Round Double Integer) reads the content of the IN parameter as a Floating -point number and converts it to a double integer (32-bit).

The result is the closest integer number ("Round to nearest").

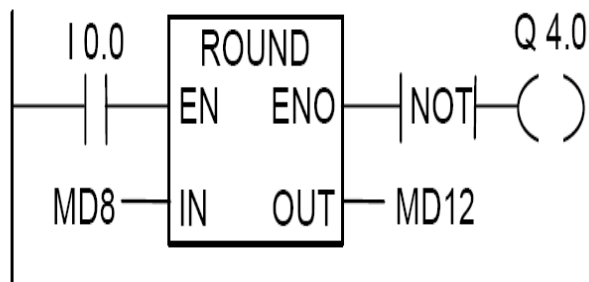
If the floating-point number lies between two integers, the even number is returned. The result is output by the parameter OUT.

If an overflow occurred ENO will be "0".

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	-	-	X	X	0	X	X	1

Example



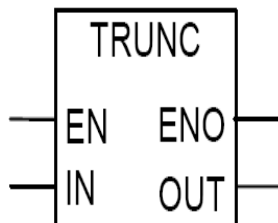
If I0.0 is "1", then the content of MD8 is read as a floating-point number and converted to the closest double integer.

The result of this "Round to nearest" function is stored in MD12.

The output Q4.0 is "1" if an overflow occurred or the instruction was not executed (I0.0 = 0).

3.14 TRUNC Truncate Double Integer Part

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D	Floating-point value to convert
OUT	DINT	I, Q, M, L, D	Whole number part of IN value

Description

TRUNC (Truncate Double Integer) reads the content of the IN parameter as a floating-point number and converts it to a double integer (32-bit).

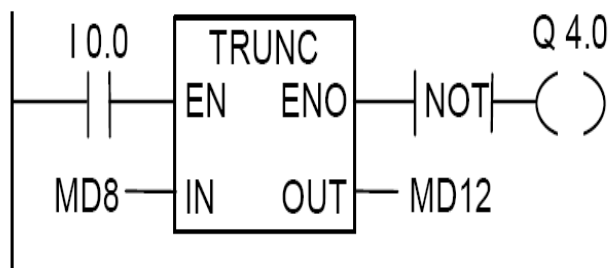
The double integer result of the ("Round to zero mode ") is output by the parameter OUT.

If an overflow occurred, ENO will be "0".

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	-	-	x	x	0	x	x	1

Example



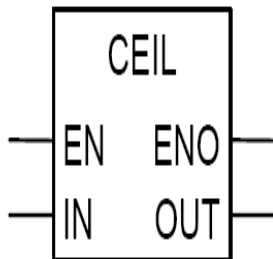
If I0.0 is "1", then the content of MD8 is read as a real number and converted to a double integer.

The integer part of the floating-point number is the result and is stored in MD12.

The output Q4.0 is "1" if an overflow occurred, or the instruction was not executed (I0.0 = 0).

3.15 CEIL Ceiling

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D	Floating-point value to convert
OUT	DINT	I, Q, M, L, D	Lowest greater double integer

Description

CEIL (Ceiling) reads the contents of the IN parameter as a floating-point number and converts it to a double integer (32-bit).

The result is the lowest integer which is greater than the floating-point number ("Round to + infinity"). If an overflow occurs, ENO will be "0".

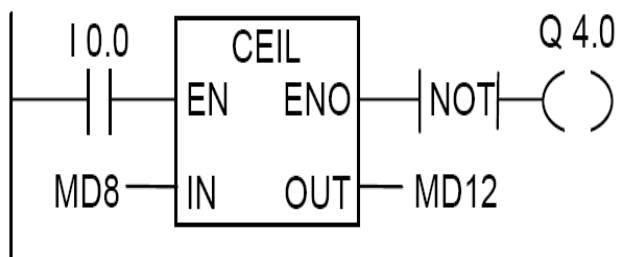
Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes*:	X	-	-	X	X	0	X	X	1
writes**:	0	-	-	-	-	0	0	0	1

* Function is executed (EN = 1)

** Function is not executed (EN = 0)

Example



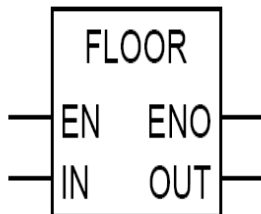
If I0.0 is 1, the contents of MD8 are read as a floating-point number which is converted into a double integer using the function **Round**.

The result is stored in MD12.

The output Q4.0 is "1" if an overflow occurred or the instruction was not processed (I0.0 = 0).

3.16 FLOOR Floor

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D	Floating-point value to convert
OUT	DINT	I, Q, M, L, D	Greatest lower double integer

Description

FLOOR (Floor) reads the content of the IN parameter as a floating-point number and converts it to a double integer (32-bit).

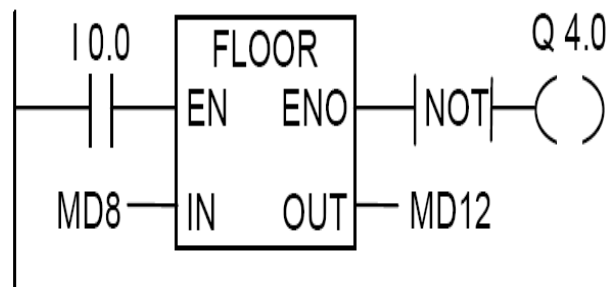
The result is the greatest integer component which is lower than the floating-point number ("Round to - infinity").

If an overflow occurred ENO will be "0".

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	-	-	X	X	0	X	X	1

Example



If I0.0 is "1", then the content of MD8 is read as a floating-point number and converted to a double integer by the round to - infinity mode.

The result is stored in MD12.

The output Q4.0 is "1" if an overflow occurred, or the instruction was not executed (I0.0 = 0).

4 Counter Instructions

4.1 Overview of Counter Instructions

Area in Memory

Counters have an area reserved for them in the memory of your CPU.

This memory area reserves one 16-bit word for each counter address.

The ladder logic instruction set supports 256 counters.

The counter instructions are the only functions that have access to the counter memory area.

Count Value

Bits 0 through 9 of the counter word contain the count value in binary code.

The count value is moved to the counter word when a counter is set.

The range of the count value is 0 to 999.

You can vary the count value within this range by using the following counter

instructions:

- S_CUD Up-Down Counter
- S_CD Down Counter
- S_CU Up Counter
- ---(SC) Set Counter Coil

- ---(CU) Up Counter Coil
- ---(CD) Down Counter Coil

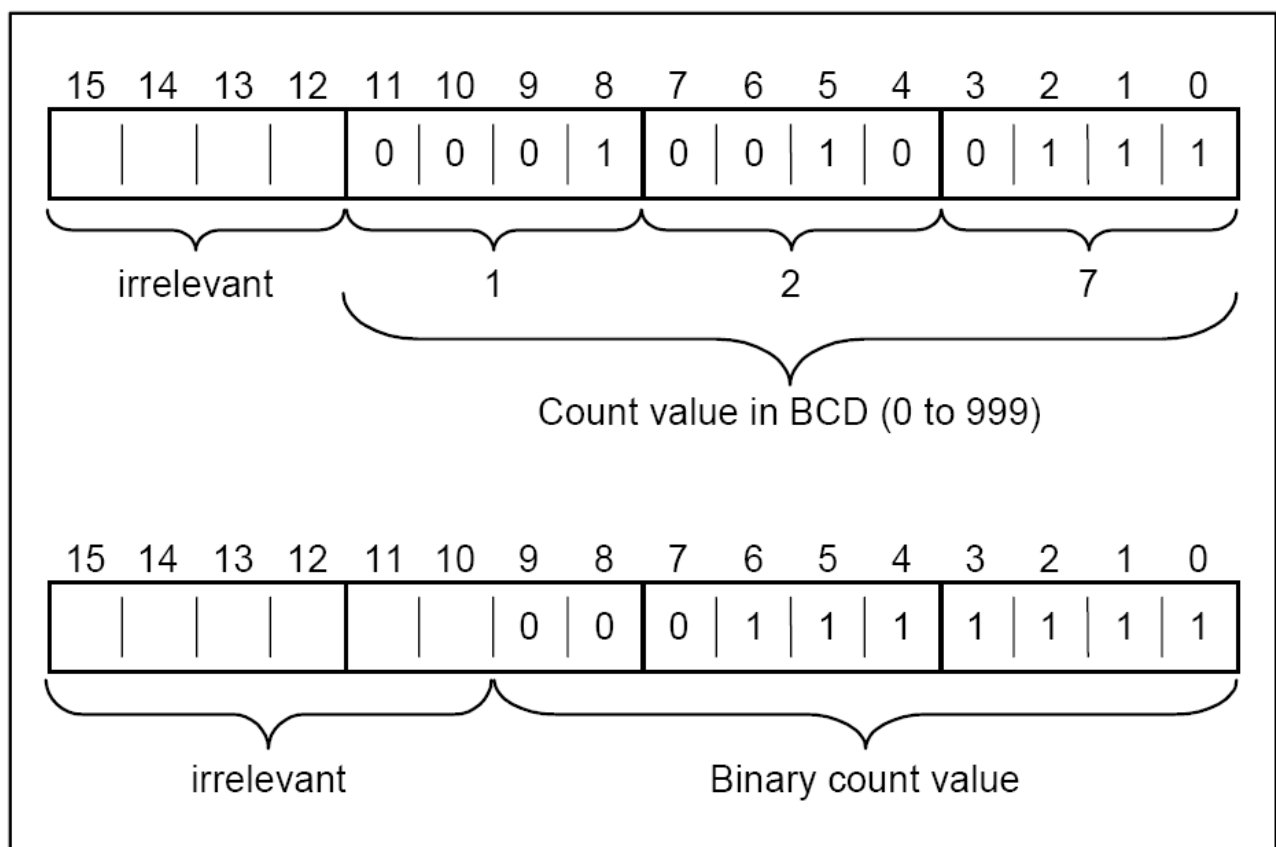
Bit Configuration in the Counter

You provide a counter with a preset value by entering a number from 0 to 999, for example 127, in the following format: C#127.

The C# stands for binary coded decimal format (BCD format: each set of four bits contains the binary code for one decimal value).

Bits 0 through 11 of the counter contain the count value in binary coded decimal format.

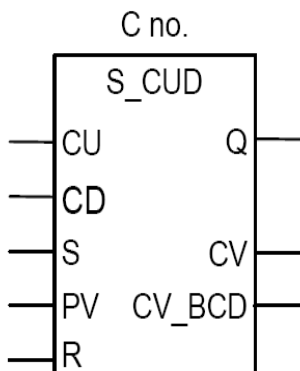
The following figure shows the contents of the counter after you have loaded the count value 127, and the contents of the counter cell after the counter has been set.



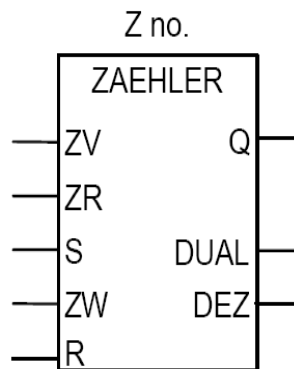
4.2 S_CUD Up-Down Counter

Symbol

English



German



Parameter English	Parameter German	Data Type	Memory Area	Description
C no.	Z no.	COUNTER	C	Counter identification number; range depends on CPU
CU	ZV	BOOL	I, Q, M, L, D	Count up input
CD	ZR	BOOL	I, Q, M, L, D	Count down input
S	S	BOOL	I, Q, M, L, D	Set input for presetting counter
PV	ZW	WORD	I, Q, M, L, D or constant	Enter counter value as C#<value> in the range from 0 to 999
PV	ZW	WORD	I, Q, M, L, D	Value for presetting counter
R	R	BOOL	I, Q, M, L, D	Reset input
CV	DUAL	WORD	I, Q, M, L, D	Current counter value, hexadecimal number
CV_BCD	DEZ	WORD	I, Q, M, L, D	Current counter value, BCD coded
Q	Q	BOOL	I, Q, M, L, D	Status of the counter

Description

S_CUD (Up-Down Counter) is preset with the value at input PV if there is a positive edge at input S.

If there is a 1 at input R, the counter is reset and the count is set to zero.

The counter is incremented by one if the signal state at input CU changes from "0" to "1" and the value of the counter is less than "999".

The counter is decremented by one if there is a positive edge at input CD and the value of the counter is greater than "0".

If there is a positive edge at both count inputs, both instructions are executed and the count value remains unchanged.

If the counter is set and if RLO = 1 at the inputs CU/CD, the counter will count accordingly in the next scan cycle, even if there was no change from a positive to a negative edge or viceversa .

The signal state at output Q is "1" if the count is greater than zero and "0" if the count is equal to zero.

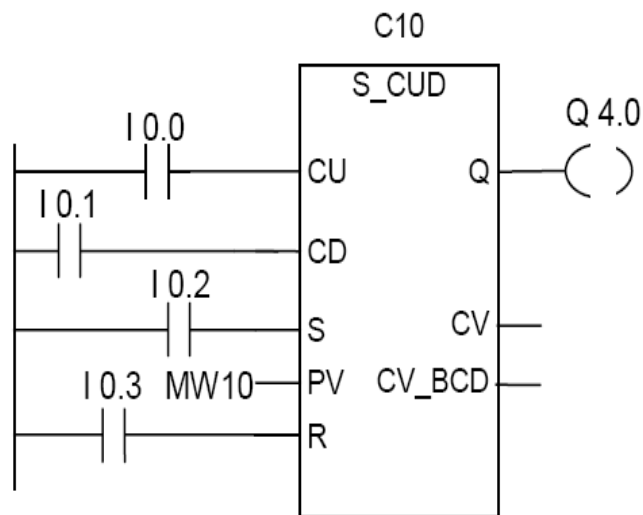
Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	x	x	x	1

Note

Avoid to use a counter at several program points (risk of counting errors).

Example



If I0.2 changes from "0" to "1", the counter is preset with the value of MW10.

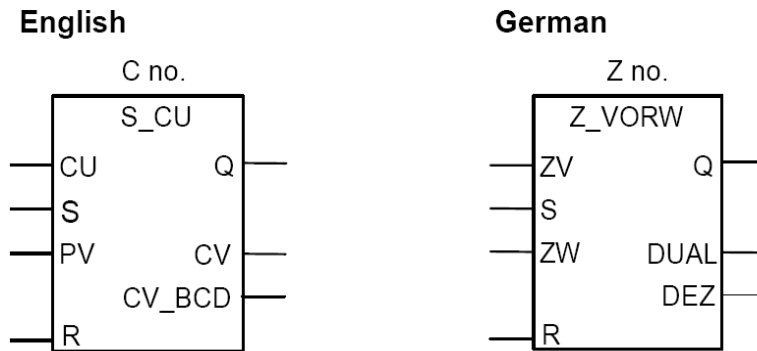
If the signal state of I0.0 changes from "0" to "1", the value of counter C10 will be incremented by one - except when the value of C10 is equal than "999".

If I0.1 changes from "0" to "1", C10 is decremented by one - except when the value of C10 is equal to "0".

Q4.0 is "1" if C10 is not equal to zero.

4.3 S_CU Up Counter

Symbol



Parameter English	Parameter German	Data Type	Memory Area	Description
C no.	Z no.	COUNTER	C	Counter identification number; range depends of CPU
CU	ZV	BOOL	I, Q, M, L, D	Count up input
S	S	BOOL	I, Q, M, L, D	Set input for presetting counter
PV	ZW	WORD	I, Q, M, L, D or constant	Enter counter value as C#<value> in the range from 0 to 999
PV	ZW	WORD	I, Q, M, L, D	Value for presetting counter
R	R	BOOL	I, Q, M, L, D	Reset input
CV	DUAL	WORD	I, Q, M, L, D	Current counter value, hexadecimal number
CV_BCD	DEZ	WORD	I, Q, M, L, D	Current counter value, BCD coded
Q	Q	BOOL	I, Q, M, L, D	Status of the counter

Description

S_CU (Up Counter) is preset with the value at input PV if there is a positive edge at input S.

The counter is reset if there is a "1" at input R and the count value is then

set to zero.

The counter is incremented by one if the signal state at input CU changes from "0" to "1" and the value of the counter is less than "999".

If the counter is set and if RLO = 1 at the inputs CU, the counter will count accordingly in the next scan cycle, even if there was no change from a positive to a negative edge or viceversa.

The signal state at output Q is "1" if the count is greater than zero and "0" if the count is equal to zero.

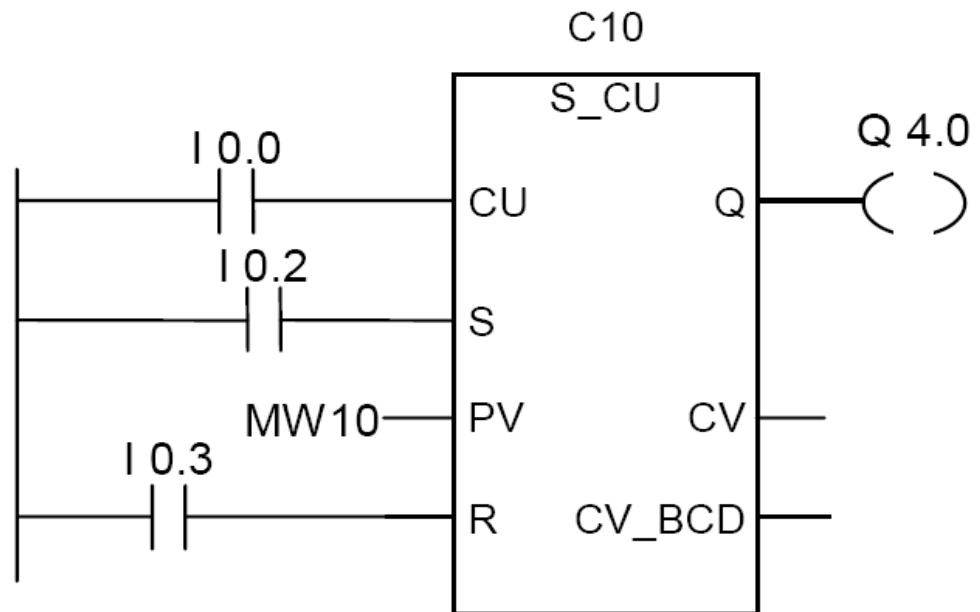
Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Note

Avoid to use a counter at several program points (risk of counting errors).

Example



If I0.2 changes from "0" to "1", the counter is preset with the value of MW10.

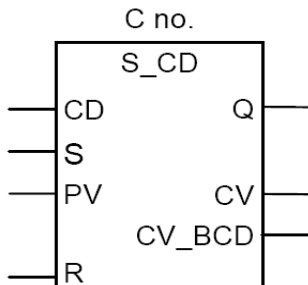
If the signal state of I0.0 changes from "0" to "1", the value of counter C10 will be incremented by one - unless the value of C10 is equal to "999".

Q4.0 is "1" if C10 is not equal to zero.

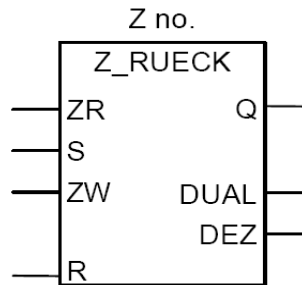
4.4 S_CD Down Counter

Symbol

English



German



Parameter English	Parameter German	Data Type	Memory Area	Description
C no.	Z no.	COUNTER	C	Counter identification number; range depends of CPU
CD	ZR	BOOL	I, Q, M, L, D	Count down input
S	S	BOOL	I, Q, M, L, D	Set input for presetting counter
PV	ZW	WORD	I, Q, M, L, D or constant	Enter counter value as C#<value> in the range from 0 to 999
PV	ZW	WORD	I, Q, M, L, D	Value for presetting counter
R	R	BOOL	I, Q, M, L, D	Reset input
CV	DUAL	WORD	I, Q, M, L, D	Current counter value, hexadecimal number
CV_BCD	DEZ	WORD	I, Q, M, L, D	Current counter value, BCD coded
Q	Q	BOOL	I, Q, M, L, D	Status counter

Description

S_CD (Down Counter) is set with the value at input PV if there is a positive edge at input S.

The counter is reset if there is a 1 at input R and the count value is then set to zero.

The counter is decremented by one if the signal state

at input CD changes from "0"

to "1" and the value of the counter is greater than zero.

If the counter is set and if RLO = 1 at the inputs CD, the counter will count accordingly in the next scan cycle, even if there was no change from a positive to a negative edge or viceversa. The signal state at output Q is "1" if the count is greater than zero and "0" if the count is equal to zero.

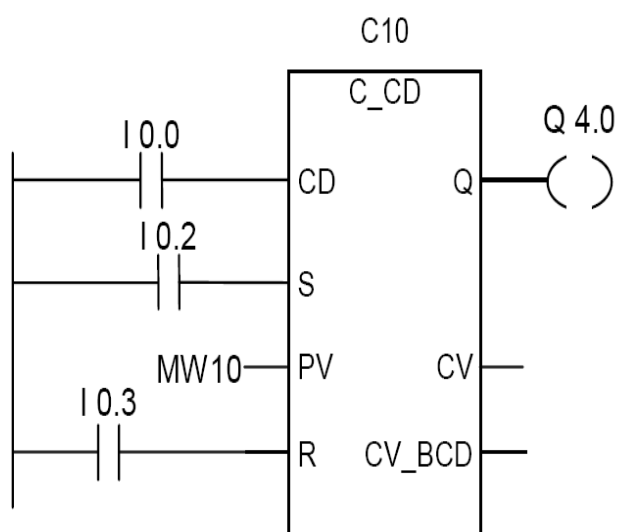
Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	x	x	x	1

Note

Avoid to use a counter at several program points (risk of counting errors).

Example



If I0.2 changes from "0" to "1", the counter is preset with the value of MW10.

If the signal state of I0.0 changes from "0" to "1", the value of counter C10 will be decremented by one - unless the value of C10 is equal to "0".

Q4.0 is "1" if C10 is not equal to zero.

4.5 ---(SC) Set Counter Value

Symbol

English

German

<C no . >

<Z no . >

---(SC)

---(SZ)

<preset

<preset value>

value >

Description

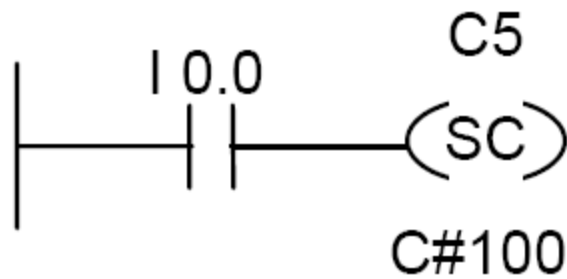
---(SC) (Set Counter Value) executes only if there is a positive edge in RLO.

At that time, the preset value transferred into the specified counter.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	-	-	-	-	0	X	-	0

Example



The counter C5 is preset with the value of 100 if there is a positive edge at input I0.0 (change from "0" to "1").

If there is no positive edge, the value of counter C5 remains unchanged.

4.6 ---(CU) Up Counter Coil

Symbol

English German

< C no . > < Z no . >

---(CU) ---(ZV)

Parameter English	Parameter German	Data Type	Memory Area	Description
<C no.>	<Z no.>	COUNTER	C	Counter identification number; range depends on CPU

Description

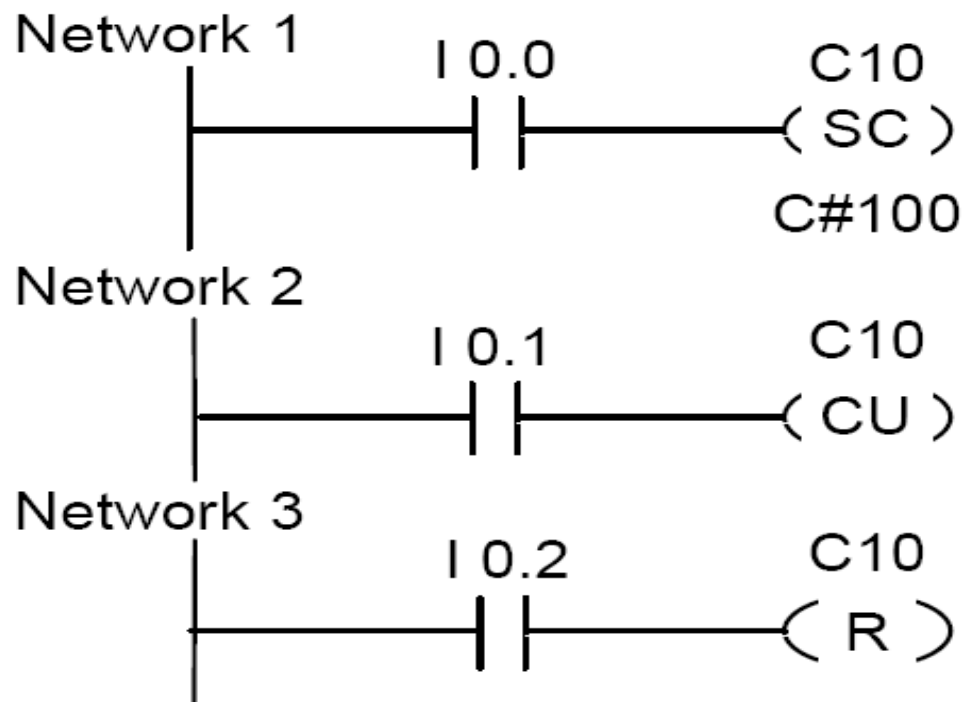
---(CU) (Up Counter Coil) increments the value of the specified counter by one if there is a positive edge in the RLO and the value of the counter is less than "999".

If there is no positive edge in the RLO or the counter already has the value "999", the value of the counter will be unchanged.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	-	-	0

Example



If the signal state of input I0.0 changes from "0" to "1" (positive edge in RLO), the preset value of 100 is loaded to counter C10.

If the signal state of input I0.1 changes from "0" to "1" (positive edge in RLO), counter C10 count value will be incremented by one unless the value of C10 is equal to "999".

If there is no positive edge in RLO, the value of C10 will be unchanged.

If the signal state of I0.2 is "1", the counter C10 is reset to "0".

4.7 ---(CD) Down Counter Coil

Symbol

English German

<C no.> <Z no.>

---(CD) ---(ZD)

Parameter English	Parameter German	Data Type	Memory Area	Description
<C no.>	<Z no.>	COUNTER	C	Counter identification number; range depends on CPU

Description

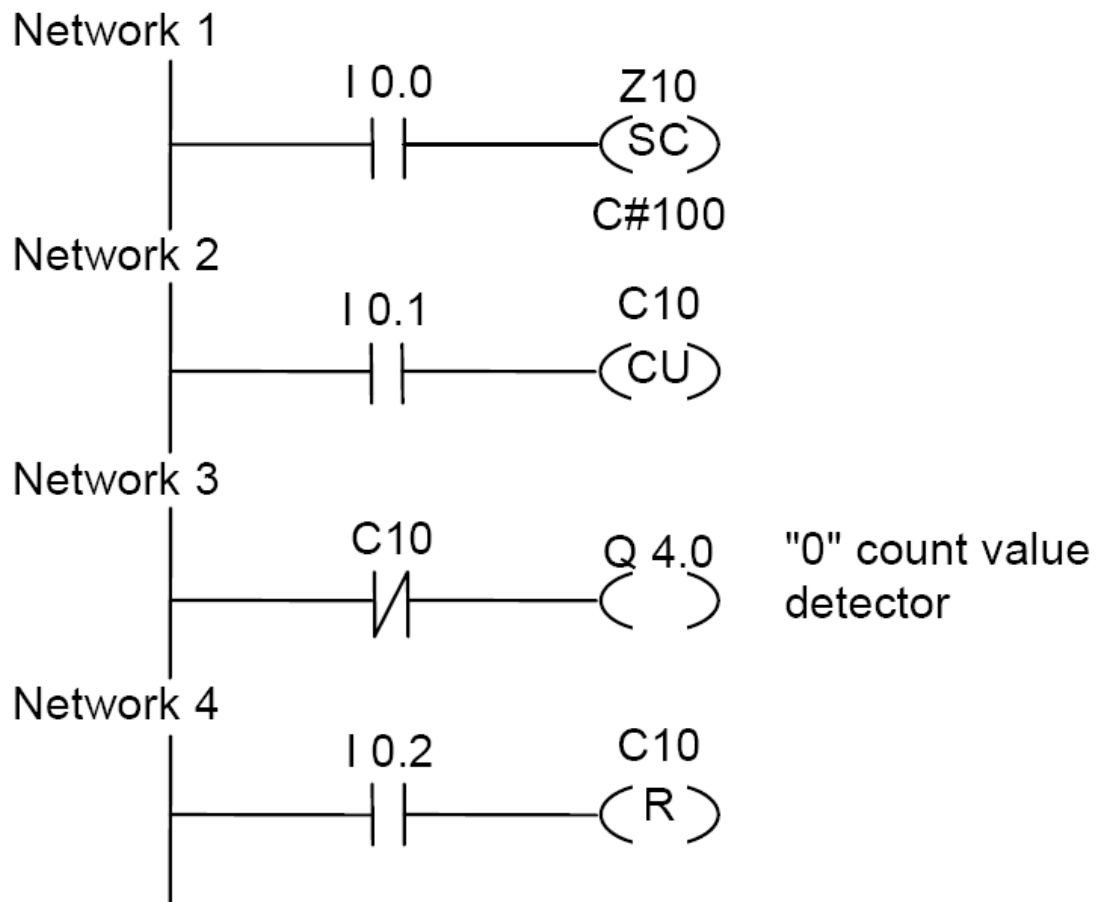
---(CD) (Down Counter Coil) decrements the value of the specified counter by one, if there is a positive edge in the RLO state and the value of the counter is more than "0".

If there is no positive edge in the RLO or the counter has already the value "0", the value of the counter will be unchanged.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	-	-	0

Example



If the signal state of input I0.0 changes from "0" to "1" (positive edge in RLO), the preset value of 100 is loaded to counter C10.

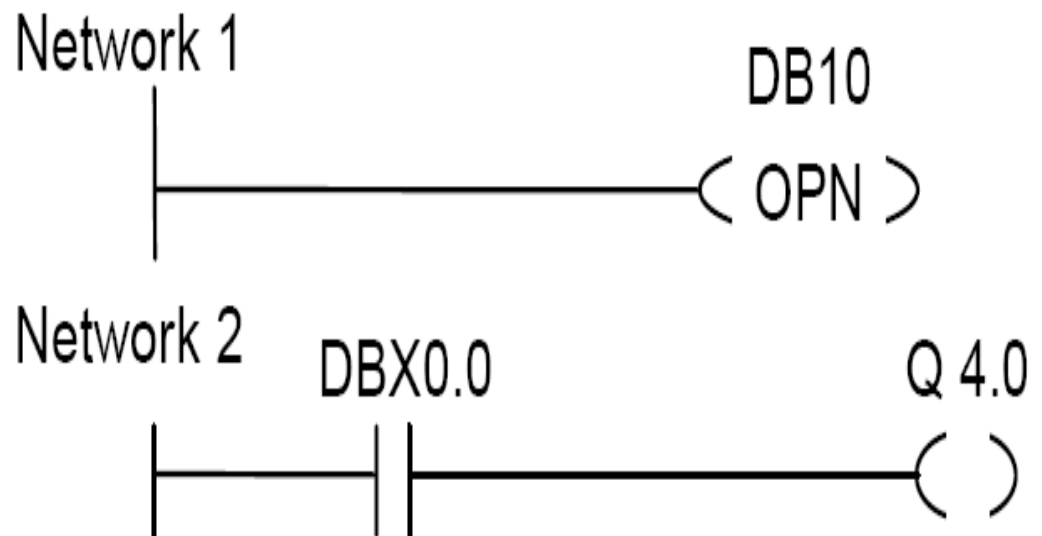
If the signal state of input I0.1 changes from "0" to "1" (positive edge in RLO), counter C10 count value will be decremented by one unless the value of C10 is equal to "0".

If there is no positive edge in RLO, the value of C10 will be unchanged.

If the count value = 0, then Q4.0 is turned on.

If the signal state of input I0.2 is "1", the counter C10 is reset to "0".

Example



Data block 10 (DB10) is opened.

The contact address (DBX0.0) refers to bit zero of data byte zero of the current data record contained in DB10.

The signal state of this bit is assigned to the output Q4.0.

6 Logic Control Instructions

6.1 Overview of Logic Control Instructions

Description

You can use logic control instructions in all logic blocks:

organization blocks (OBs),
function blocks (FBs), and functions (FCs).

There are logic control instructions to perform the following functions:

- ---(JMP)--- Unconditional Jump
- ---(JMP)--- Conditional Jump
- ---(JMPN)--- Jump-If-Not

Label as Address

The address of a Jump instruction is a label.

A label consists of a maximum of four characters.

The first character must be a letter of the alphabet; the other characters can be letters or numbers (for example, SEG3).

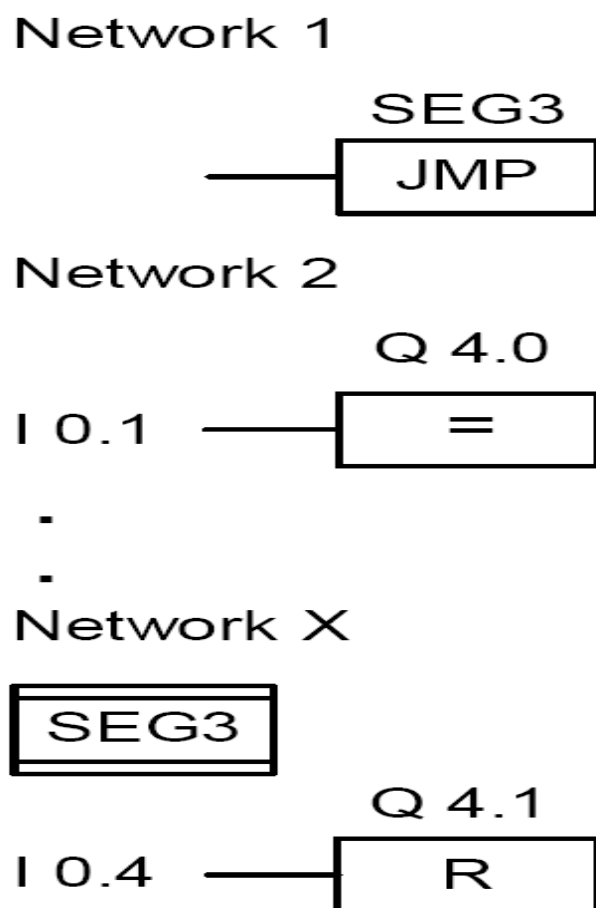
The jump label indicates the destination to which you want the program to jump.

Label as Destination

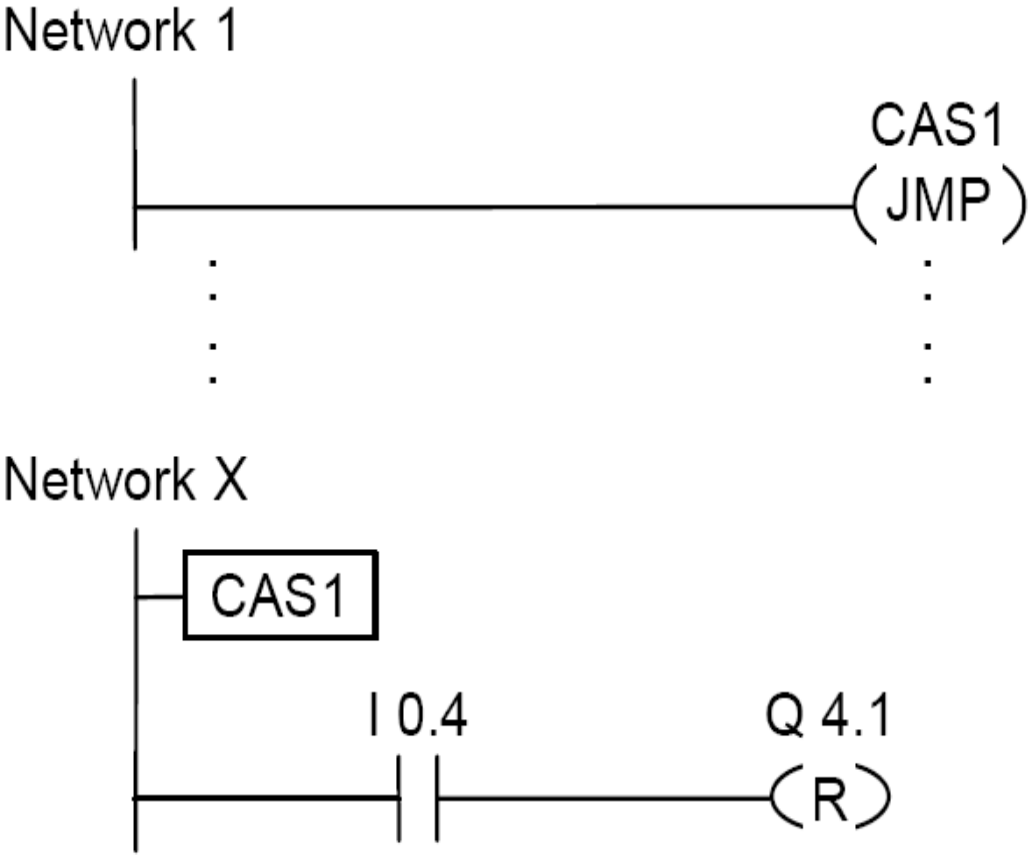
The destination label must be at the beginning of a network.

You enter the destination label at the beginning of the network by selecting LABEL from the ladder logic browser.

An empty box appears. In the box, you type the name of the Label.



Example



The jump is always executed and the instructions between the jump instruction and the jump label are missed out.

6.3 ---(**JMP**)--- Conditional Jump

Symbol

<label name>

---(**JMP**)

Description

---(**JMP**) (jump within the block when 1) functions as a conditional jump when the RLO of the previous logic operation is "1".

A destination (LABEL) must also exist for every ---(**JMP**).

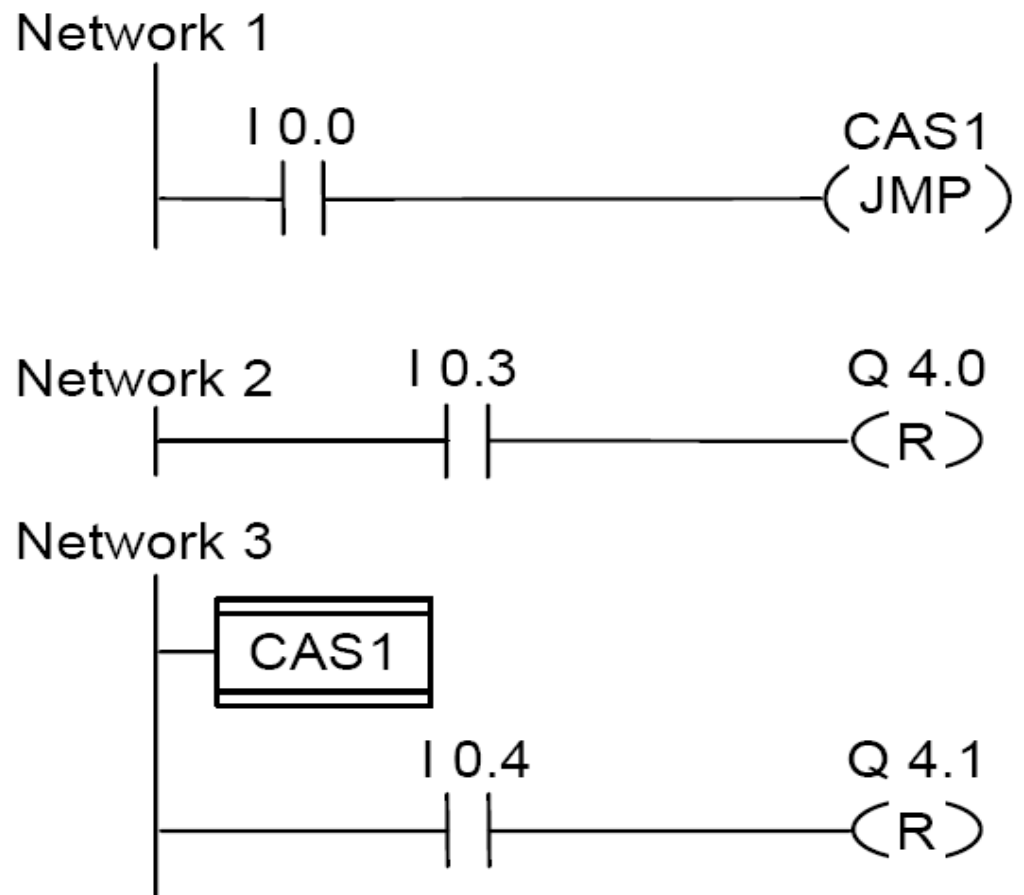
All instructions between the jump instruction and the label are not executed.

If a conditional jump is not executed, the RLO changes to "1" after the jump Instruction .

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	1	1	0

Example



If **I 0.0 = "1"**, the jump to label **CAS1** is executed. Because of the jump, the instruction to reset output **Q4.0** is not executed even if there is a logic "1" at **I 0.3**.

6.4 ---(JMPN) Jump-If-Not

Symbol

<label name>

---(JMPN)

Description

---(JMPN) (Jump-If-not) corresponds to a "goto label" function which is executed if the RLO is "0".

A destination (LABEL) must also exist for every ---(JMPN).

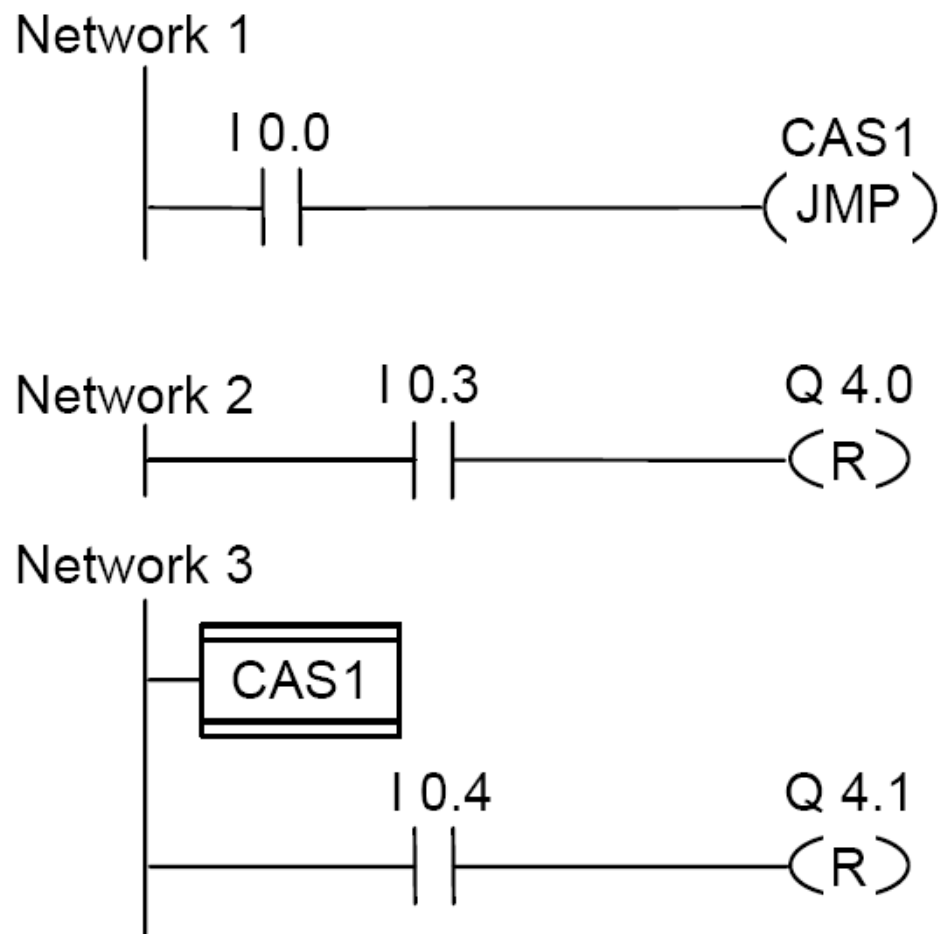
All instructions between the jump instruction and the label are not executed.

If a conditional jump is not executed, the RLO changes to "1" after the jump instruction.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	1	1	0

Example



If I0.0 = "0", the jump to label CAS1 is executed. Because of the jump, The instruction to reset output Q4.0 is not executed even if there is a logic "1" at I0.3.

6.5 LABEL Label

Symbol



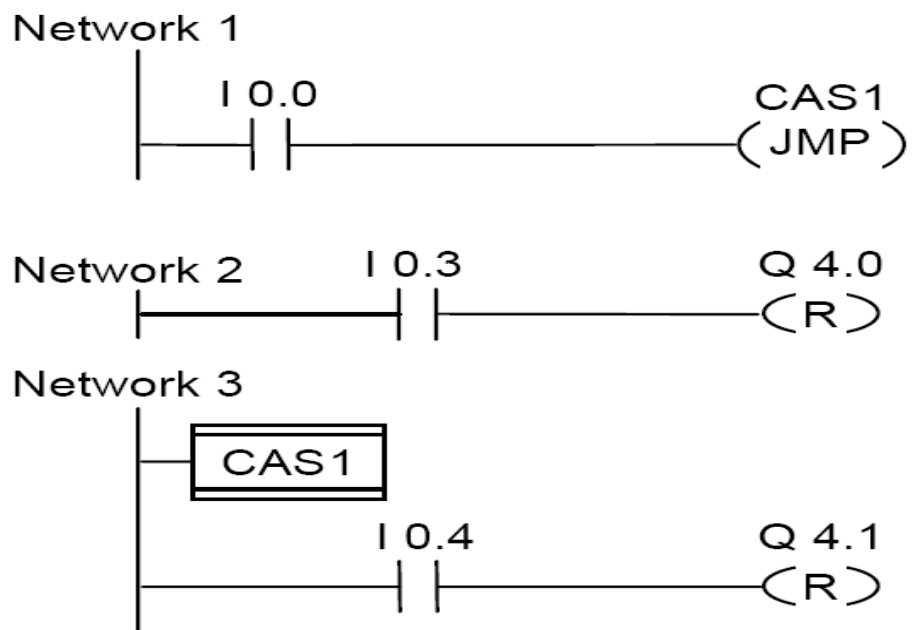
Description

LABEL is the identifier for the destination of a jump instruction.

The first character must be a letter of the alphabet; the other characters can be letters or numbers (for example, CAS1).

A jump label (**LABEL**) must exist for every ---(JMP) or ---(JMPN).

Example



If I0.0 = "1", the jump to label CAS1 is executed.

Because of the jump, the instruction to reset output Q4.0 is not executed even if there is a logic "1" at I0.3.

7 Integer Math Instructions

7.1 Overview of Integer Math

Instructions

Description

Using integer math, you can carry out the following operations with two integer numbers (16 and 32 bits):

- **ADD_I** Add Integer
- **SUB_I** Subtract Integer
- **MUL_I** Multiply Integer
- **DIV_I D** ivate Integer
- **ADD_DI** Add Double Integer
- **SUB_DI** Subtract Double Integer
- **MUL_DI** Multiply Double Integer
- **DIV_DI** Divide Double Integer
- **MOD_DI** Return Fraction Double Integer

7.2 Evaluating the Bits of the Status Word with Integer Math Instructions :

Description

The integer math instructions affect the following bits in the Status word:

CC1 and CC0, OV and OS.

The following tables show the signal state of the bits in the status word for the results of instructions with Integers (16 and 32 bits):

Valid Range for the Result	CC 1	CC 0	OV	OS
0 (zero)	0	0	0	*
16 bits: $-32\,768 \leq \text{result} < 0$ (negative number) 32 bits: $-2\,147\,483\,648 \leq \text{result} < 0$ (negative number)	0	1	0	*
16 bits: $32\,767 \geq \text{result} > 0$ (positive number) 32 bits: $2\,147\,483\,647 \geq \text{result} > 0$ (positive number)	1	0	0	*

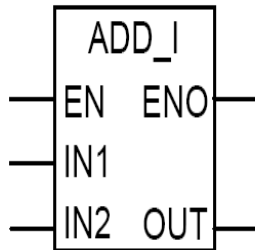
* The OS bit is not affected by the result of the instruction.

Invalid Range for the Result	A1	A0	OV	OS
Underflow (addition) 16 bits: result = -65536 32 bits: result = -4 294 967 296	0	0	1	1
Underflow (multiplication) 16 bits: result < -32 768 (negative number) 32 bits: result < -2 147 483 648 (negative number)	0	1	1	1
Overflow (addition, subtraction) 16 bits: result > 32 767 (positive number) 32 bits: result > 2 147 483 647 (positive number)	0	1	1	1
Overflow (multiplication, division) 16 bits: result > 32 767 (positive number) 32 bits: result > 2 147 483 647 (positive number)	1	0	1	1
Underflow (addition, subtraction) 16 bits: result < -32. 768 (negative number) 32 bits: result < -2 147 483 648 (negative number)	1	0	1	1
Division by 0	1	1	1	1

Operation	A1	A0	OV	OS
+D: result = -4 294 967 296	0	0	1	1
/D or MOD: division by 0	1	1	1	1

7.3 ADD_I Add Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	INT	I, Q, M, L, D or constant	First value for addition
IN2	INT	I, Q, M, L, D or constant	Second value for addition
OUT	INT	I, Q, M, L, D	Result of addition

Description

ADD_I (Add Integer) is activated by a logic "1" at the Enable (EN) Input. IN1 and IN2 are added and the result can be scanned at OUT.

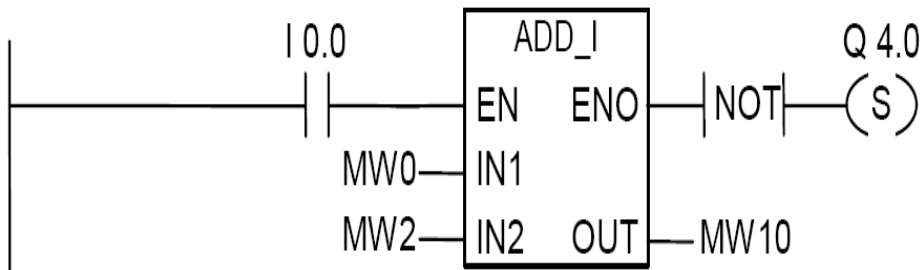
If the result is outside the permissible range for an integer (16-bit), the OV bit and OS bit will be "1" and ENO is logic "0", so that other functions after this math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word with Integer Math Instructions.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



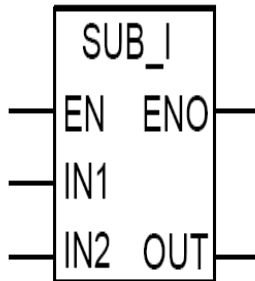
The ADD_I box is activated if I0.0 = "1".

The result of the addition MW0 + MW2 is output to MW10.

If the result was outside the permissible range for an integer, the output Q4.0 is set.

7.4 SUB_I Subtract Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	INT	I, Q, M, L, D or constant	First value for subtraction
IN2	INT	I, Q, M, L, D or constant	Value to subtract
OUT	INT	I, Q, M, L, D	Result of subtraction

Description

SUB_I (Subtract Integer) is activated by a logic "1" at the Enable (EN) Input.

IN2 is subtracted from IN1 and the result can be scanned at OUT.

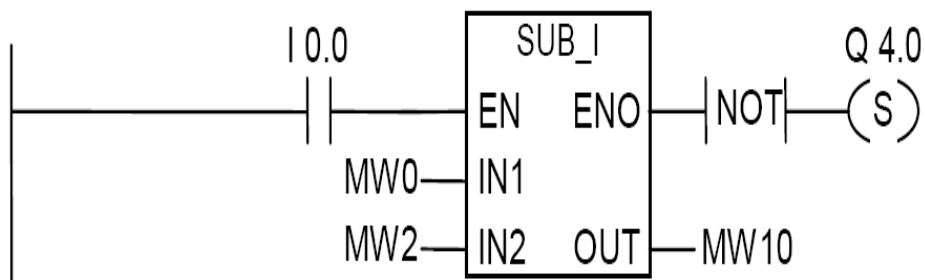
If the result is outside the permissible range for an integer (16-bit), the OV bit and OS bit will be "1" and ENO is logic "0", so that other functions after this math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word with Integer Math Instructions.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



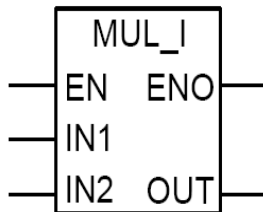
The SUB_I box is activated if I0.0 = "1".

The result of the subtraction MW0 - MW2 is output to MW10.

If the result was outside the permissible range for an integer or the signal state of I0.0 = 0, the output Q4.0 is set.

7.5 MUL_I Multiply Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	INT	I, Q, M, L, D or constant	First value for multiplication
IN2	INT	I, Q, M, L, D or constant	Second value for multiplication
OUT	INT	I, Q, M, L, D	Result of multiplication

Description

MUL_I (Multiply Integer) is activated by a logic "1" at the Enable (EN) Input.

IN1 and IN2 are multiplied and the result can be scanned at OUT.

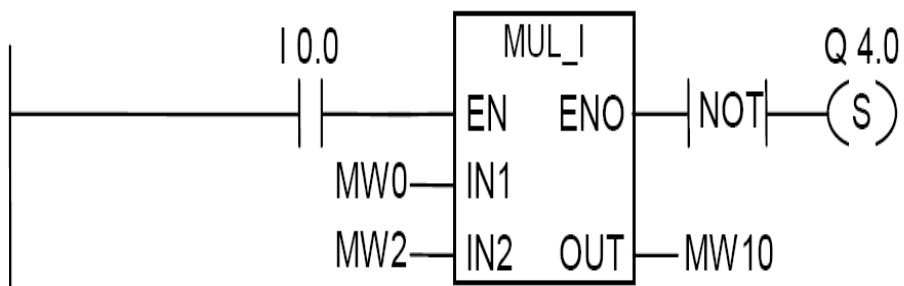
If the result is outside the permissible range for an integer (16-bit), the OV bit and OS bit will be "1" and ENO is logic "0", so that other functions after this math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word with Integer Math Instructions.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example

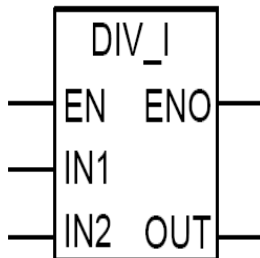


The MUL_I box is activated if I0.0 = "1". The result of the multiplication MW0 x MW2 is output to MD10.

If the result was outside the permissible range for an integer, the output Q4.0 is set.

7.6 DIV_I Divide Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	INT	I, Q, M, L, D or constant	Dividend
IN2	INT	I, Q, M, L, D or constant	Divisor
OUT	INT	I, Q, M, L, D	Result of division

Description

DIV_I (Divide Integer) is activated by a logic "1" at the Enable (EN) Input.

IN1 is divided by IN2 and the result can be scanned at OUT.

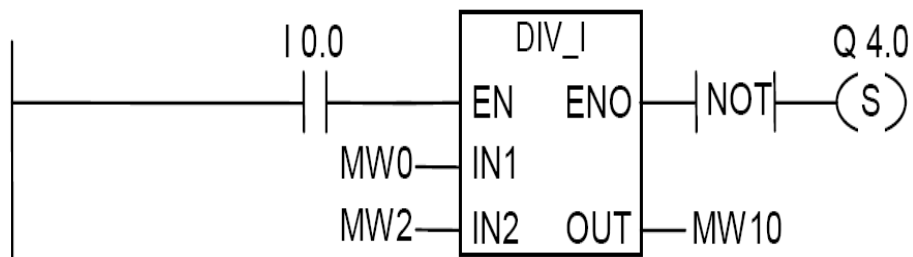
If the result is outside the permissible range for an integer (16-bit), the OV bit and OS bit is "1" and ENO is logic "0", so that other functions after this math box which are connected by ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word with Integer Math Instructions.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

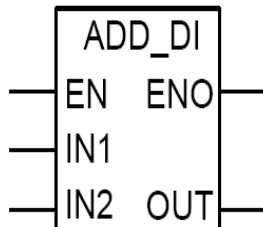
Example



The DIV_I box is activated if I0.0 = "1". The result of the division MW0 by MW2 is output to MW10. If the result was outside the permissible range for an integer, the output Q4.0 is set.

7.7 ADD_DI Add Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	DINT	I, Q, M, L, D or constant	First value for addition
IN2	DINT	I, Q, M, L, D or constant	Second value for addition
OUT	DINT	I, Q, M, L, D	Result of addition

Description

ADD_DI (Add Double Integer) is activated by a logic "1" at the Enable (EN) Input.

IN1 and IN2 are added and the result can be scanned at OUT.

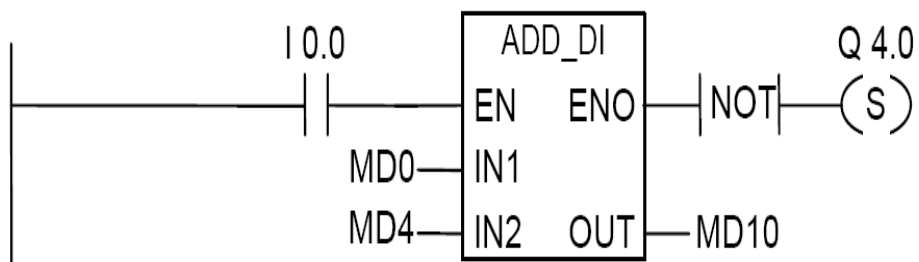
If the result is outside the permissible range for a double integer (32-bit), the OV bit and OS bit will be "1" and ENO is logic "0", so that other functions after this math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word with Integer Math Instructions.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



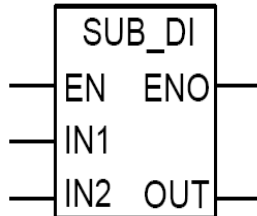
The ADD_DI box is activated if I0.0 = "1".

The result of the addition MD0 + MD4 is output to MD10.

If the result was outside the permissible range for a double integer, the output Q4.0 is set.

7.8 SUB_DI Subtract Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	DINT	I, Q, M, L, D or constant	First value for subtraction
IN2	DINT	I, Q, M, L, D or constant	Value to subtract
OUT	DINT	I, Q, M, L, D	Result of subtraction

Description

SUB_DI (Subtract Double Integer) is activated by a logic "1" at the Enable (EN) Input.

IN2 is subtracted from IN1 and the result can be scanned at OUT.

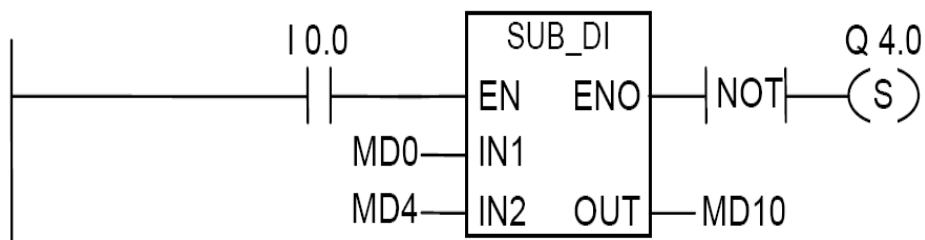
If the result is outside the permissible range for a double integer (32-bit), the OV bit and OS bit will be "1" and ENO is logic "0", so that other functions after this math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word with Integer Math Instructions.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



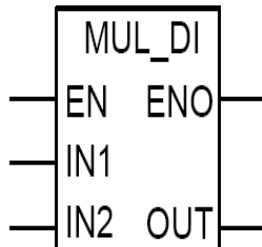
The SUB_DI box is activated if I0.0 = "1".

The result of the subtraction MD0 - MD4 is output to MD10.

If the result was outside the permissible range for a double integer, the output Q4.0 is set.

7.9 MUL_DI Multiply Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	DINT	I, Q, M, L, D or constant	First value for multiplication
IN2	DINT	I, Q, M, L, D or constant	Second value for multiplication
OUT	DINT	I, Q, M, L, D	Result of multiplication

Description

MUL_DI (Multiply Double Integer) is activated by a logic "1" at the Enable (EN) Input. IN1 and IN2 are multiplied and the result can be scanned at OUT.

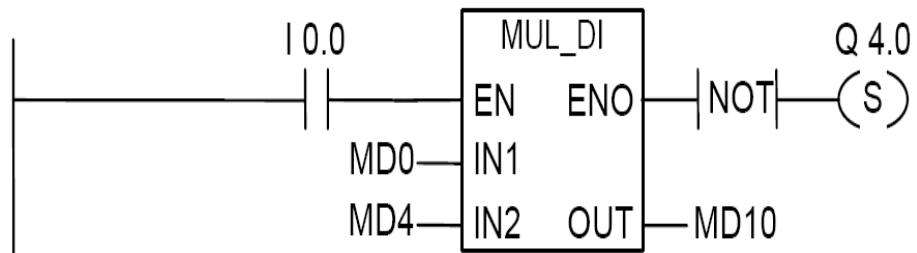
If the result is outside the permissible range for a double integer (32-bit), the OV bit and OS bit will be "1" and ENO is logic "0", so that other functions after this math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word with Integer Math Instructions.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



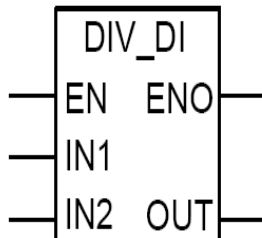
The MUL_DI box is activated if I0.0 = "1".

The result of the multiplication MD0 x MD4 is output to MD10.

If the result was outside the permissible range for a double integer, the output Q4.0 is set.

7.10 DIV_DI Divide Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	DINT	I, Q, M, L, D or constant	Dividend
IN2	DINT	I, Q, M, L, D or constant	Divisor
OUT	DINT	I, Q, M, L, D	Whole-number result of division

Description

DIV_DI (Divide Double Integer) is activated by a logic "1" at the Enable (EN) Input.

IN1 is divided by IN2 and the result can be scanned at OUT.

The Divide Double Integer element does not produce a remainder.

If the result is outside the permissible range for a double integer (32-bit), the OV bit and OS bit is "1" and ENO is logic "0", so that other functions after this

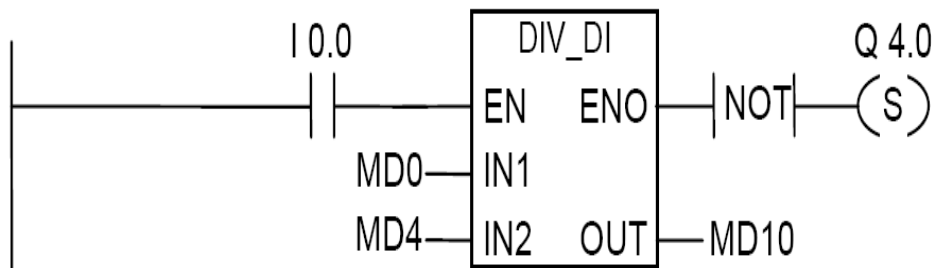
math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word with Integer Math Instructions.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



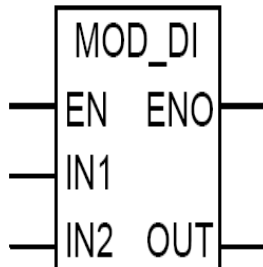
The DIV_DI box is activated if I0.0 = "1".

The result of the division MD0 : MD4 is output to MD10.

If the result was outside the permissible range for a double integer, the output Q4.0 is set.

7.11 MOD_DI Return Fraction Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	DINT	I, Q, M, L, D or constant	Dividend
IN2	DINT	I, Q, M, L, D or constant	Divisor
OUT	DINT	I, Q, M, L, D	Remainder of division

Description

MOD_DI (Return Fraction Double Integer) is activated by a logic "1" at the Enable (EN) Input. IN1 is divided by IN2 and the fraction can be scanned at OUT.

If the result is outside the permissible range for a double integer (32-bit), the OV bit and OS bit is "1" and ENO is logic "0", so that other functions after this

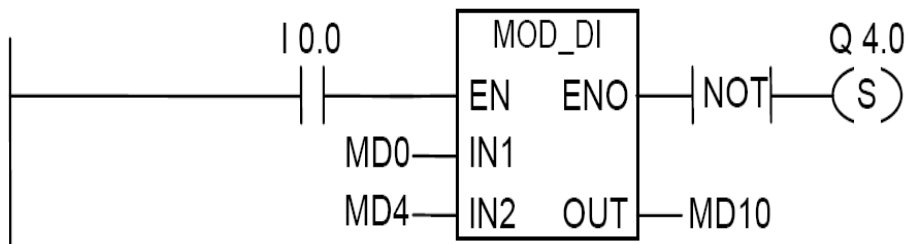
math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word with Integer Math Instructions.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



The DIV_DI box is activated if I0.0 = "1".

The remainder of the division MD0:MD4 is output to MD10.

If the remainder was outside the permissible range for a double integer, the output Q4.0 is set .

8 Floating Point Math Instructions

8.1 Overview of Floating-Point Math Instruction

Description

The IEEE 32-bit floating-point numbers belong to the data type called REAL.

You can use the floating-point math instructions to perform the following math instructions using two 32-bit IEEE floating-point numbers:

- **ADD_R Add Real**
- **SUB_R Subtract Real**
- **MUL_R Multiply Real**
- **DIV_R Divide Real**

**Using floating-point math,
you can carry out the following operations
with one 32-bit IEEE floating-point number:**

- **Establish the Absolute Value (ABS)**
- **Establish the Square (SQR) and the Square Root (SQRT)**
- **Establish the Natural Logarithm (LN)**
- **Establish the Exponential Value (EXP) to base e (= 2,71828)**
- **Establish the following trigonometrical functions of an angle represented as a 32-bit IEEE floating-point number**
 - **Sine (SIN) and Arc Sine (ASIN)**
 - **Cosine (COS) and Arc Cosine (ACOS)**
 - **Tangent (TAN) and Arc Tangent (ATAN) See also Evaluating the Bits of the Status Word.**

8.2 Evaluating the Bits of the Status Word with Floating-Point Math Instructions

Description

Floating-point instructions affect the following bits in the status word:

CC 1 and CC 0, OV and OS.

The following tables show the signal state of the bits in the status word for the results of instructions with floating-point numbers (32 bits):

Valid Area for a Result	CC 1	CC 0	OV	OS
+0, -0 (zero)	0	0	0	*
$-3.402823\text{E}+38 < \text{result} < -1.175494\text{E}-38$ (negative number)	0	1	0	*
$+1.175494\text{E}-38 < \text{result} < 3.402824\text{E}+38$ (positive number)	1	0	0	*

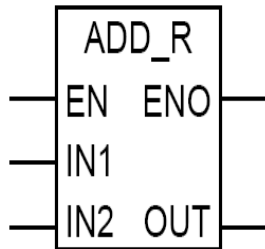
* The OS bit is not affected by the result of the instruction.

Invalid Area for a Result	CC 1	CC 0	OV	OS
Underflow $-1.175494\text{E}-38 < \text{result} < -1.401298\text{E}-45$ (negative number)	0	0	1	1
Underflow $+1.401298\text{E}-45 < \text{result} < +1.175494\text{E}-38$ (positive number)	0	0	1	1
Overflow Result $< -3.402823\text{E}+38$ (negative number)	0	1	1	1
Overflow Result $> 3.402823\text{E}+38$ (positive number)	1	0	1	1
Not a valid floating-point number or illegal instruction (input value outside the valid range)	1	1	1	1

8.3 Basic Instructions

8.3.1 ADD_R Add Real

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	REAL	I, Q, M, L, D or constant	First value for addition
IN2	REAL	I, Q, M, L, D or constant	Second value for addition
OUT	REAL	I, Q, M, L, D	Result of addition

Description

ADD_R (Add Real) is activated by a logic "1" at the Enable (EN) Input.

IN1 and IN2 are added and the result can be scanned at OUT.

If the result is outside the permissible range for a floating-point number (overflow or underflow), the OV bit and OS bit will be "1" and ENO is "0", so

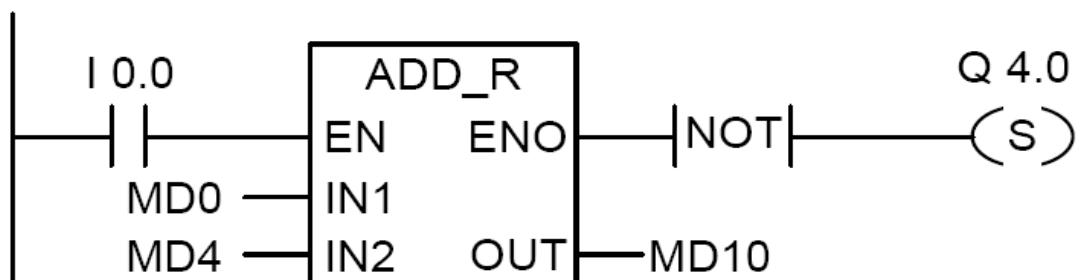
that other functions after this math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	X	0	X	X	1

Example



The ADD_R box is activated by logic "1" at I0.0.

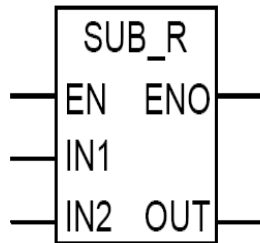
The result of the addition MD0 + MD4 is output to MD10.

If the result was outside the permissible range for a floating-point number or if the program statement was not processed

(I0.0 = 0), the output Q4.0 is set.

8.3.2 SUB_R Subtract Real

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	REAL	I, Q, M, L, D or constant	First value for subtraction
IN2	REAL	I, Q, M, L, D or constant	Value to subtract
OUT	REAL	I, Q, M, L, D	Result of subtraction

Description

SUB_R (Subtract Real) is activated by a logic "1" at the Enable (EN) Input.

IN2 is subtracted from IN1 and the result can be scanned at OUT.

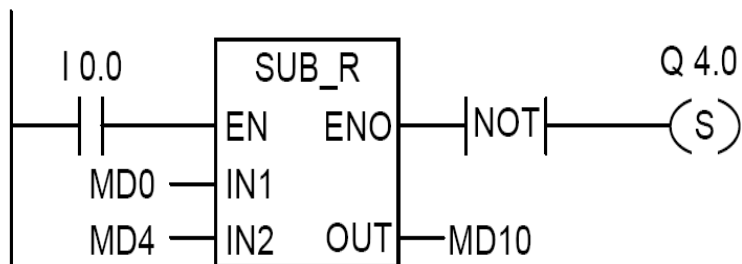
If the result is outside the permissible range for a floating-point number (overflow or underflow), the OV bit and OS bit will be "1" and ENO is logic "0", so that other functions after this math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



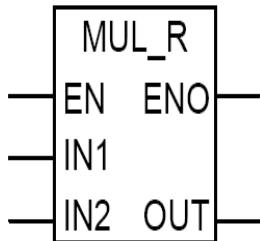
The SUB_R box is activated by logic "1" at I0.0.

The result of the subtraction MD0 - MD4 is output to MD10.

If the result was outside the permissible range for a floating-point number or if the program statement was not processed, the output Q4.0 is set.

8.3.3 MUL_R Multiply Real

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	REAL	I, Q, M, L, D or constant	First value for multiplication
IN2	REAL	I, Q, M, L, D or constant	Second value for multiplication
OUT	REAL	I, Q, M, L, D	Result of multiplication

Description

MUL_R (Multiply Real) is activated by a logic "1" at the Enable (EN) Input.

IN1 and IN2 are multiplied and the result can be scanned at OUT.

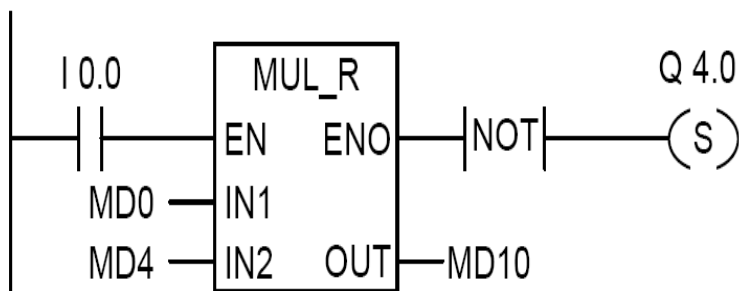
If the result is outside the permissible range for a floating-point number (overflow or underflow), the OV bit and OS bit will be "1" and ENO is logic "0", so that other functions after this math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



The MUL_R box is activated by logic "1" at I0.0.

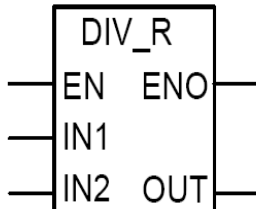
The result of the multiplication MD0 x MD4 is output to MD0.

If the result was outside the permissible range for a floating-point number or if the program statement was not processed, the output

Q4.0 is set.

8.3.4 DIV_R Divide Real

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	REAL	I, Q, M, L, D or constant	Dividend
IN2	REAL	I, Q, M, L, D or constant	Divisor
OUT	REAL	I, Q, M, L, D	Result of division

Description

DIV_R (Divide Real) is activated by a logic "1" at the Enable (EN) Input.

IN1 is divided by IN2 and the result can be scanned at OUT.

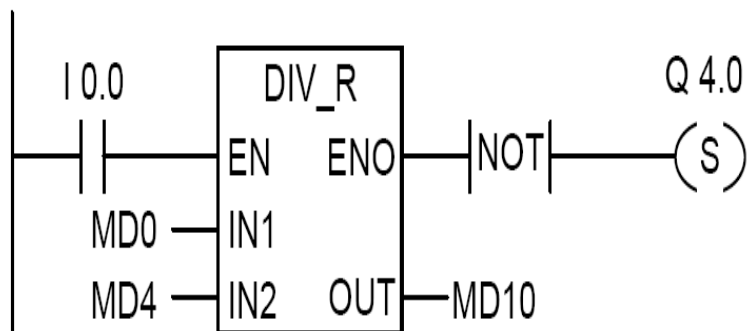
If the result is outside the permissible range for a floating-point number (overflow or underflow), the OV bit and OS bit is "1" and ENO is logic "0", so that other functions after this math box which are connected by the ENO (cascade arrangement) are not executed.

See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

Example



The DIV_R box is activated by logic "1" at I0.0.

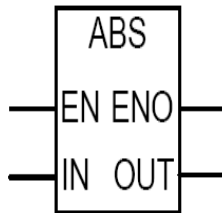
The result of the division MD0 by MD4 is output to MD10.

If the result was outside the permissible range for a floating-point number or if the program statement was not processed, the output

Q4.0 is set.

8.3.5 ABS Establish the Absolute Value of a Floating-Point Number

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: absolute value of the floating-point number

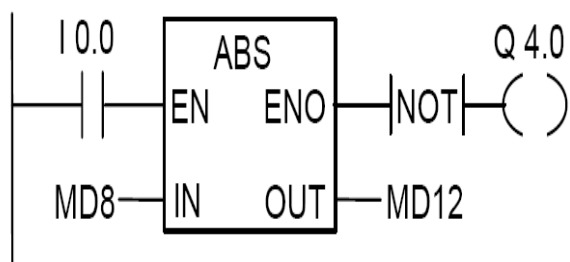
Description

ABS establishes the absolute value of a floating-point number.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	-	-	-	-	0	1	1	1

Example



If I0.0 = "1", the absolute value of MD8 is output at MD12.

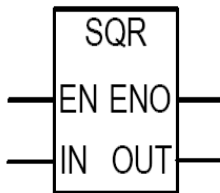
MD8 = + 6.234 gives MD12 = 6.234.

Output Q4.0 is "1" when the conversion is not executed (ENO = EN = 0).

8.4 Extended Instructions

8.4.1 SQR Establish the Square

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: square of floating-point number

Description

SQR establishes the square of a floating-point number.

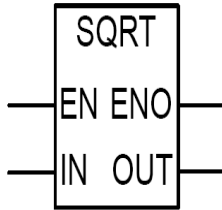
See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	X	0	X	X	1

8.4.2 SQRT Establish the Square Root

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: square root of floating-point number

Description

SQRT establishes the square root of a floating-point number.

This instruction issues a positive result when the address is greater than "0".

Sole exception:

The square root of -0 is -0.

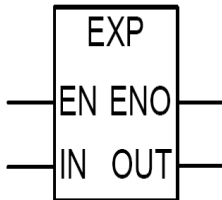
See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

8.4.3 EXP Establish the Exponential Value

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: exponential value of the floating-point number

Description

EXP establishes the exponential value of a floating-point number on the basis e ($=2,71828\dots$).

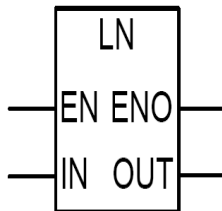
See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	X	0	X	X	1

8.4.4 LN Establish the Natural Logarithm

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: natural logarithm of the floating-point number

Description

LN establishes the natural logarithm of a floating-point number.

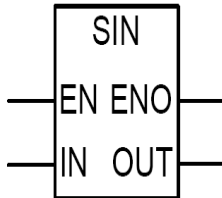
See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	X	0	X	X	1

8.4.5 SIN Establish the Sine Value

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: sine of the floating-point number

Description

SIN establishes the sine value of a floating-point number. The floating-point number represents an angle in a radian measure here.

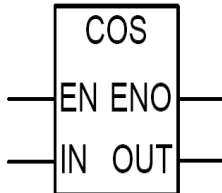
See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	X	0	X	X	1

8.4.6 COS Establish the Cosine Value

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: cosine of the floating-point number

Description

COS establishes the cosine value of a floating-point number.

The floating-point number represents an angle in a radian measure here.

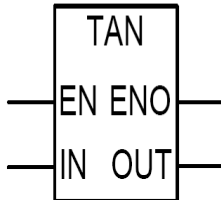
See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	X	0	X	X	1

8.4.7 TAN Establish the Tangent Value

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: tangent of the floating-point number

Description

TAN establishes the tangent value of a floating-point number.

The floating-point number represents an angle in a radian measure here.

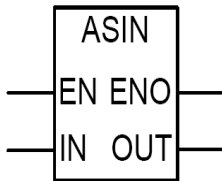
See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	X	0	X	X	1

8.4.8 ASIN Establish the Arc Sine Value

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: arc sine of the floating-point number

Description

ASIN establishes the arc sine value of a floating-point number with a definition range $-1 \leq \text{input value} \leq 1$. The result represents an angle in a radian measure

within the range

$$-\pi/2 \leq \text{output value} \leq +\pi/2$$

where $\pi = 3.1415\dots$

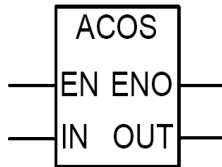
See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

8.4.9 ACOS Establish the Arc Cosine Value

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: arc cosine of the floating-point number

Description

ACOS establishes the arc cosine value of a floating-point number

with a definition

range $-1 \leq \text{input value} \leq 1$.

The result represents an angle in a radian measure within the range

$0 \leq \text{output value} \leq +\pi$

where $\pi = 3.1415\dots$

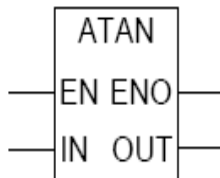
See also Evaluating the Bits of the Status Word.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

8.4.10 ATAN Establish the Arc Tangent Value

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	REAL	I, Q, M, L, D or constant	Input value: floating-point
OUT	REAL	I, Q, M, L, D	Output value: arc tangent of the floating-point number

Description

ATAN establishes the arc tangent value of a floating-point number. The result represents an angle in a radian measure within the range

$$-\pi/2 \leq \text{output value} \leq +\pi/2$$

where $\pi = 3.1415\dots$

See also Evaluating the Bits of the Status Word.

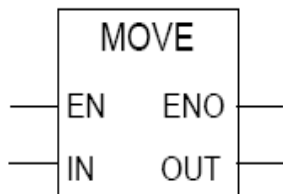
Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	x	0	x	x	1

9 Move Instructions

9.1 MOVE Assign a Value

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	All elementary data types with a length of 8, 16, or 32 bits	I, Q, M, L, D or constant	Source value
OUT	All elementary data types with a length of 8, 16, or 32 bits	I, Q, M, L, D	Destination address

Description

MOVE (Assign a Value) is activated by the Enable EN Input.

The value specified at the IN input is copied to the address specified at the OUT output. ENO has the same logic state as EN.

MOVE can copy only BYTE, WORD, or DWORD data objects.

User-defined data types like arrays or structures have to be copied with the system function "BLKMOVE" (SFC 20).

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	-	-	-	-	0	1	1	1

MCR (Master Control Relay) dependency

MCR dependency is activated only if a Move box is placed inside an active MCR zone.

Within an activated MCR zone, if the MCR is on and there is power flow to the enable input; the addressed data is copied as described above.

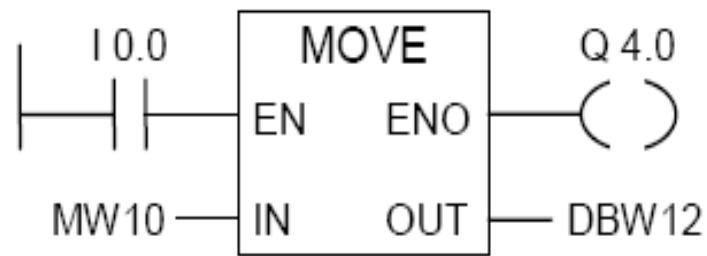
If the MCR is off, and a MOVE is executed, a logic "0" is written to the specified OUT address regardless of current IN states.

Note

When moving a value to a data type of a different length, higher-value bytes are truncated as necessary or filled up with zeros:

Example: Double Word	1111 1111	0000 1111	1111 0000	0101 0101
Move	Result			
to a double word:	1111 1111	0000 1111	1111 0000	0101 0101
to a byte:				0101 0101
to a word:			1111 0000	0101 0101
Example: Byte				1111 0000
Move	Result			
to a byte:				1111 0000
to a word:			0000 0000	1111 0000
to a double word:	0000 0000	0000 0000	0000 0000	1111 0000

Example



The instruction is executed if I0.0 is "1".

The content of MW10 is copied to data word 12 of the currently open DB.

Q4.0 is "1" if the instruction is executed.

If the example rungs are within an activated MCR zone:

- When MCR is on, MW10 data is copied to DBW12 as described above.
- When MCR is off, "0" is written to DBW12.

10 Program Control Instructions

10.1 Overview of Program Control Instructions

Description

The following program control instructions are available:

- **---(CALL) Call FC SFC from Coil (without Parameters)**
- **CALL_FB Call FB from Box**
- **CALL_FC Call FC from Box**
- **CALL_SFB Call System FB from Box**
- **CALL_SFC Call System FC from Box**
- **Call Multiple Instance**
- **Call Block from a Library**
- **Important Notes on Using MCR Functions**
- **---(MCR<) Master Control Relay On**
- **---(MCR>) Master Control Relay Off**
- **---(MCRA) Master Control Relay Activate**
- **---(MCRD) Master Control Relay Deactivate**
- **RET Return**

10.2 --- (Call) Call FC SFC from Coil (Without Parameters)

Symbol

<FC/SFC no.>

---(CALL)

Parameter	Data Type	Memory Area	Description
<FC/SFC no.>	BLOCK_FC BLOCK_SFC	-	Number of FC/SFC; range depends on CPU

Description

---(Call) (Call FC or SFC without Parameters) is used to call a function (FC) or system function (SFC) that has no passed parameters.

A call is only executed if RLO is "1" at the CALL coil.

If ---(Call) is executed,

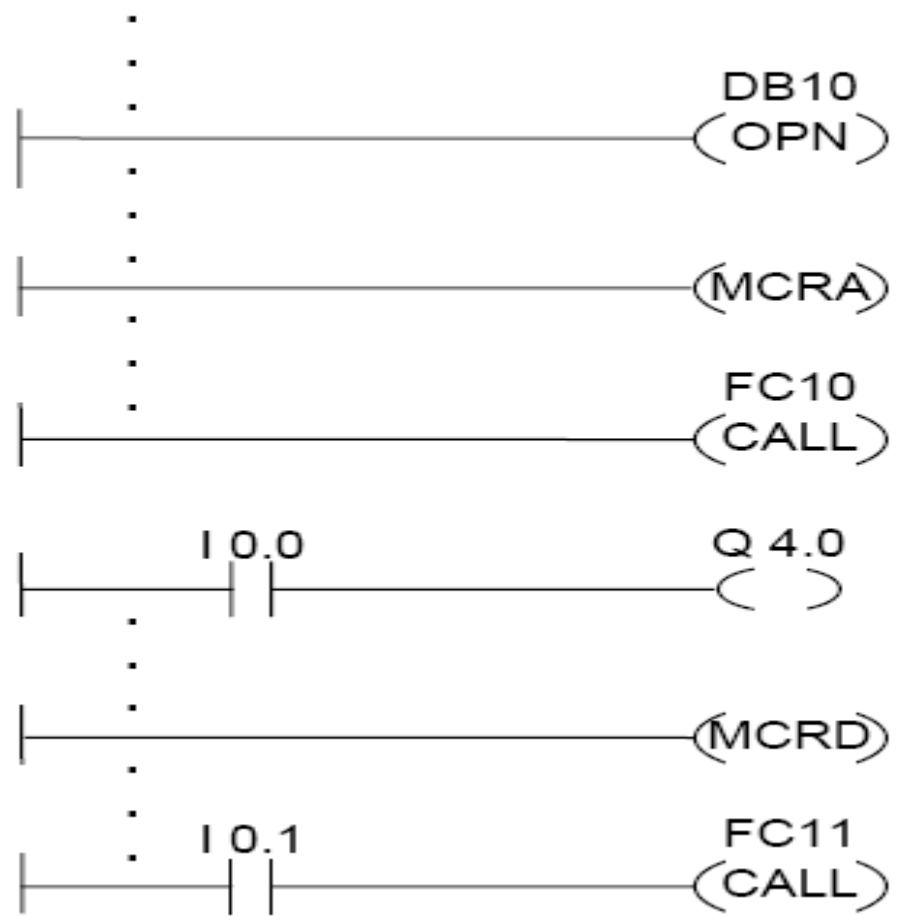
- The return address of the calling block is stored,
- The previous local data area is replaced by the current local data area,
- The MA bit (active MCR bit) is shifted to the B stack,
- A new local data area for the called function is created.

After this, program processing continues in the called FC or SFC.

Status word

		BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
Unconditional:	writes:	-	-	-	-	0	0	1	-	0
Conditional:	writes:	-	-	-	-	0	0	1	1	0

Example



The Ladder rungs shown above are program sections from a function block written by a user.

In this FB, DB10 is opened and MCR functionality is activated.

If the unconditional call of FC10 is executed, the following occurs:

The return address of the calling FB plus selection data for DB10 and for the instance data block for the calling FB are saved.

The MA bit, set to "1" in the MCRA instruction, is pushed to the B stack and then set to "0" for the called block (FC10).

Program processing continues in FC10.

If MCR functionality is required by FC10, it must be re-activated within FC10.

When FC10 is finished, program processing returns to the calling FB.

The MA bit is restored, DB10 and the instance data block for the user-written FB become the current DBs again, regardless of which DBs FC10 has used.

The program continues with the next rung by assigning the logic state of I0.0 to output Q4.0.

The call of FC11 is a conditional call.

It is only executed if I0.1 is "1".

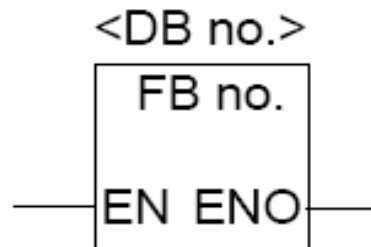
If it is executed, the process of passing program control to and returning from FC11 is the same as was described for FC10.

Note

After returning to the calling block, the previously open DB is not always open again. Please make sure you read the note in the README file.

10.3 CALL_FB Call FB from Box

Symbol



The symbol depends on the FB

(whether it has parameters and how many of them).

It must have the EN, ENO, and the name or number of the FB.

Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
FB no.	BLOCK_FB	-	Number of FB/DB; range depends on CPU
DB no.	BLOCK_DB	-	

Description

CALL_FB (Call a Function Block from a Box) executed if EN is "1".

If CALL_FB is executed,

- The return address of the calling block is stored,
- The selection data for the two current data blocks (DB and instance DB) are stored,

- The previous local data area is replaced by the current local data area,
- The MA bit (active MCR bit) is shifted to the B stack,
- A new local data area for the called function block is created.

After this, program processing continues within the called function block.

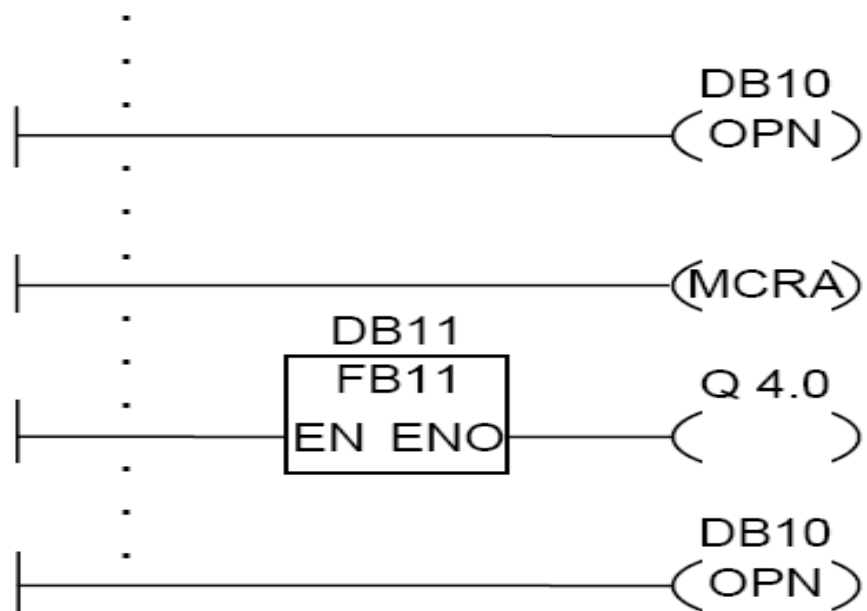
The BR bit is scanned in order to find out the ENO.

The user has to assign the required state (error evaluation) to the BR bit in the called block using ---(SAVE).

Status word

		BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
Unconditional:	writes:	x	-	-	-	0	0	x	x	x
Conditional:	writes:	-	-	-	-	0	0	x	x	x

Example



The Ladder rungs shown above are program sections from a function block written by a user.

In this FB, DB10 is opened and MCR functionality is activated.

If the unconditional call of FB11 is executed, the following occurs:

The return address of the calling FB plus selection data for DB10 and for the instance data block for the calling FB are saved.

The MA bit, set to "1" in the MCRA instruction, is pushed to the B stack and then set to "0" for the called block (FB11).

Program processing continues in FB11.

If MCR functionality is required by FB11, it must be re-activated within FB11.

The state of the RLO must be saved in the BR bit by the instruction ---(SAVE) in order to be able to evaluate errors in the calling FB.

When FB11 is finished, program processing returns to the calling FB.

The MA bit is restored and the instance data block of the user-written FB is opened again.

If the FB11 is processed correctly, ENO = "1" and therefore Q4.0 = "1".

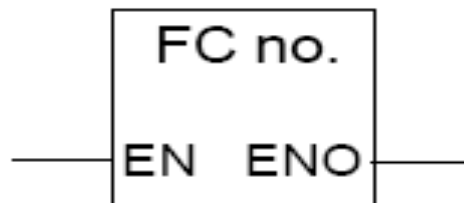
Note

When opening an FB or SFB, the number of the previously opened DB is lost.

The required DB has to be reopened.

10.4 CALL_FC Call FC from Box

Symbol



The symbol depends on the FC (whether it has parameters and how many of them). It must have EN, ENO, and the name or number of the FC.

Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
FC no.	BLOCK_FC	-	Number of FC; range depends on CPU

Description

CALL_FC (Call a Function from a Box) is used to call a function (FC).

The call is executed if EN is "1".

If CALL_FC is executed,

- The return address of the calling block is stored,
- The previous local data area is replaced by the current local data area,
- The MA bit (active MCR bit) is shifted to the B stack,

- A new local data area for the called function is created.

After this, program processing continues in the called function.

The BR bit is scanned in order to find out the ENO. The user has to assign the required state (error evaluation) to the BR bit in the called block using

---**(SAVE)**.

If you call a function and the variable declaration table of the called block has IN, OUT, and IN_OUT declarations, these variables are added in the program for the calling block as a list of formal parameters.

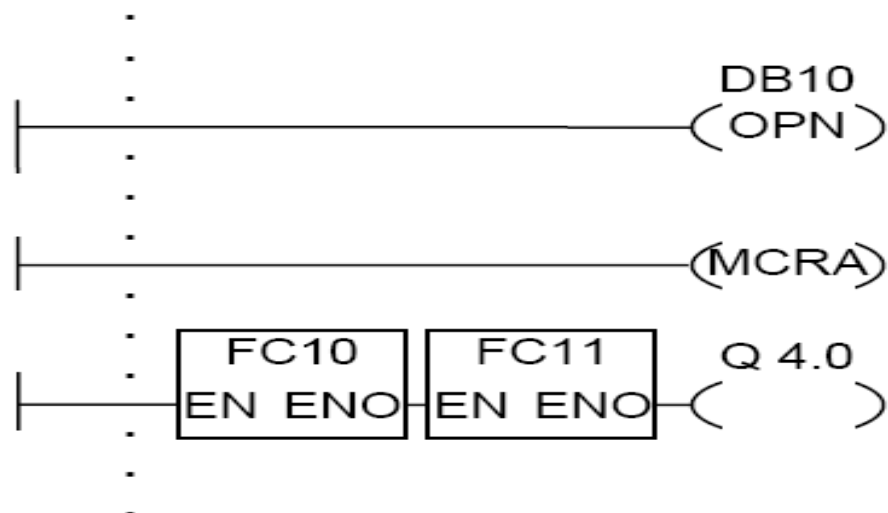
When calling the function, you **must** assign actual parameters to the formal parameters at the call location.

Any initial values in the function declaration have no significance.

Status word

		BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
Unconditional:	writes:	x	-	-	-	0	0	x	x	x
Conditional:	writes:	-	-	-	-	0	0	x	x	x

Example



The Ladder rungs shown above are program sections from a function block written by a user. In this FB, DB10 is opened and MCR functionality is activated.

If the unconditional call of FC10 is executed, the following occurs:

The return address of the calling FB plus selection data for DB10 and for the instance data block for the calling FB are saved. The MA bit, set to "1" in the MCRA instruction, is pushed to the B stack and then set to "0" for the called block (FC10).

Program processing continues in FC10.

If MCR functionality is required by FC10, it must be re-activated within FC10.

The state of the RLO must be saved in the BR bit by the instruction ---(SAVE) in order to be able to evaluate errors in the calling FB.

When FC10 is finished, program processing returns to the calling FB.

The MA bit is restored.

After execution of FC10, program processing is continued in the calling FB depending on the ENO:

ENO = "1" FC11 is processed

ENO = "0" processing starts in the next network

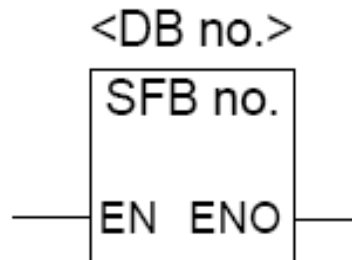
If FC11 is also processed correctly, ENO = "1" and therefore Q4.0 = "1".

Note

After returning to the calling block, the previously open DB is not always open again. Please make sure you read the note in the README file.

10.5 CALL_SFB Call System FB from Box

Symbol



The symbol depends on the SFB (whether it has parameters and how many of them). It must have the EN, ENO, and the name or number of the SFB.

Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
SFB no.	BLOCK_SFB	-	Number of SFB; range depends on CPU
DB no.	BLOCK_DB	-	

Description

CALL_SFB

(Call a System Function Block from a Box) is executed if EN is "1".

If CALL_SFB is executed,

- The return address of the calling block is stored,

- The selection data for the two current data blocks (DB and instance DB) are stored,
- The previous local data area is replaced by the current local data area,
- The MA bit (active MCR bit) is shifted to the B stack,
- A new local data area for the called system function block is created.

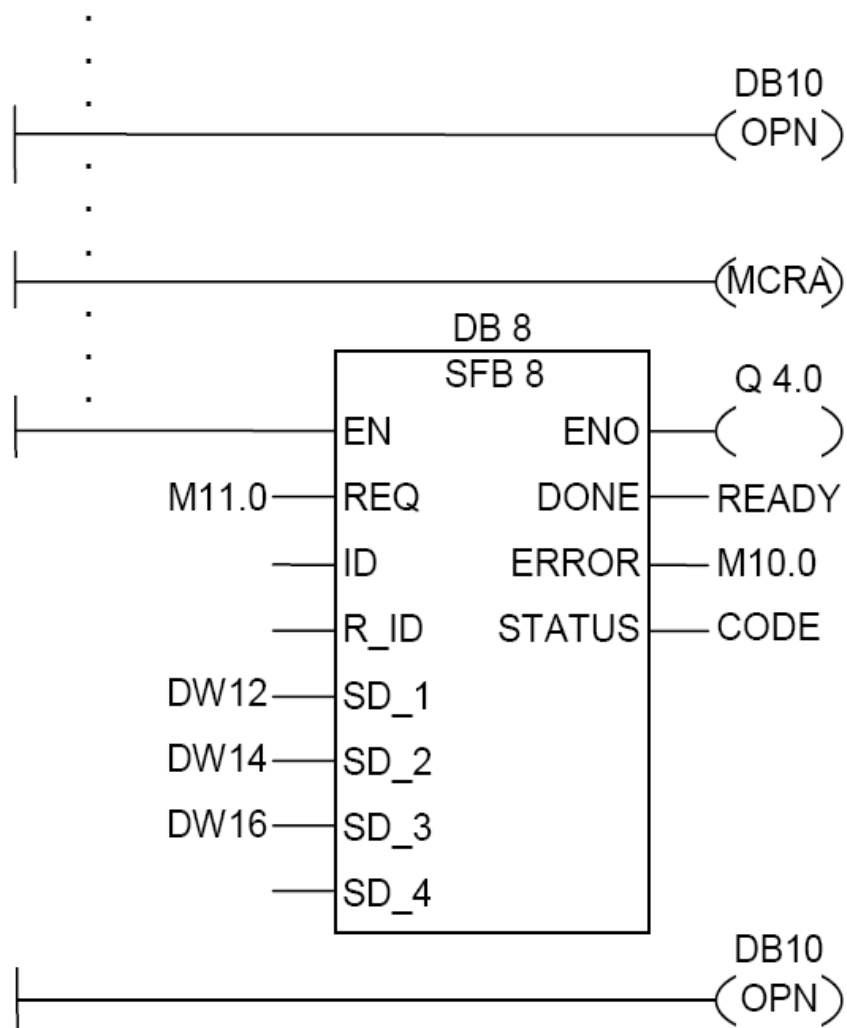
Program processing then continues in the called SFB.

ENO is "1" if the SFB was called (EN = "1") and no error occurs.

Status word

		BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
Unconditional:	writes:	X	-	-	-	0	0	X	X	X
Conditional:	writes:	-	-	-	-	0	0	X	X	X

Example



The Ladder rungs shown above are program sections from a function block written by a user.

In this FB, DB10 is opened and MCR functionality is activated.

If the unconditional call of SFB8 is executed, the following occurs:

The return address of the calling FB plus selection data for DB10 and for

The instance data block for the calling FB are saved.

The MA bit, set to "1" in the MCRA instruction, is pushed to the B stack and then set to "0" for the called block (SFB8).

Program processing continues in SFB8.

When SFB8 is finished, program processing returns to the calling FB.

The MA bit is restored and the instance data block of the user-written FB becomes the current instance DB.

If the SFB8 is processed correctly, ENO = "1" and therefore Q4.0 = "1".

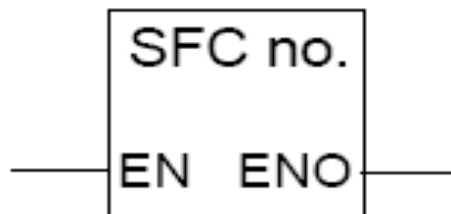
Note

When opening an FB or SFB, the number of the previously opened DB is lost.

The required DB has to be reopened.

10.6 CALL_SFC Call System FC from Box

Symbol



The symbol depends on the SFC

(whether it has parameters and how many of them).

It must have EN, ENO, and the name or number of the SFC.

Parameter	Data Type	Memory Area	Description
EN	BOOL	-	Enable input
ENO	BOOL	-	Enable output
SFC no.	BLOCK_SFC	-	Number of SFC; range depends on CPU

Description

CALL_SFC (Call a System Function from a Box) is used to call an SFC.

The call is executed if EN is "1".

If CALL_SFC is executed,

- The return address of the calling block is stored,
- The previous local data area is replaced by the current local data area,

- The MA bit (active MCR bit) is shifted to the B stack,
- A new local data area for the called system function is created.

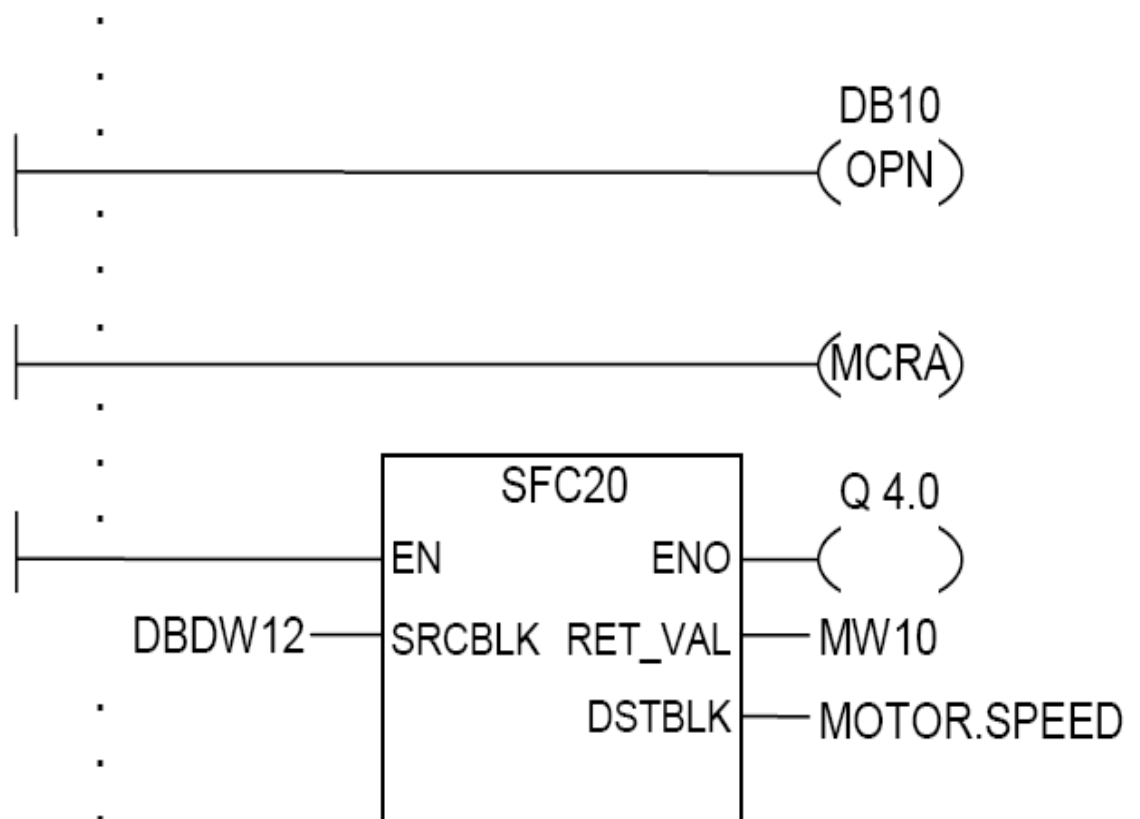
After this, program processing continues in the called SFC.

ENO is "1" if the SFC was called (EN = "1") and no error occurs.

Status word

		BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
Unconditional:	writes:	x	-	-	-	0	0	x	x	x
Conditional:	writes:	-	-	-	-	0	0	x	x	x

Example



The Ladder rungs shown above are program sections from a function block written by a user.

In this FB, DB10 is opened and MCR functionality is activated.

If the unconditional call of SFC20 is executed, the following occurs:

The return address of the calling FB plus selection data for DB10 and for the instance data block for the calling FB are saved.

The MA bit, set to "1" in the MCRA instruction, is pushed to the B stack and then set to "0" for the called block (SFC20).

Program processing continues in SFC20.

When SFC20 is finished, program processing returns to the calling FB.

The MA bit is restored.

After processing the SFC20, the program is continued in the calling FB depending on the ENO:

ENO = "1" Q4.0 = "1"

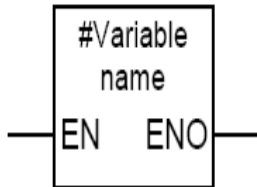
ENO = "0" Q4.0 = "0"

Note

After returning to the calling block, the previously open DB is not always open again. Please make sure you read the note in the README file.

10.7 Call Multiple Instance

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
#Variable name	FB, SFB	-	Name of multiple instance

Description

A multiple instance is created by declaring a static variable with the data type of a function block.

Only multiple instances that have already been declared are included in the program element catalog.

The symbol for a multiple instance varies depending on whether and how many parameters are present.

EN, ENO and the variable name are always present.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	0	0	x	x	x

10.8 Call Block from a Library

The libraries available in the SIMATIC Manager can be used here to select a block that

- Is integrated in your CPU operating system ("Standard Library" library for STEP 7 projects in version 3 and "stdlibs (V2)" for STEP 7 projects in version 2)
- You saved yourself in a library because you wanted to use it a number of times.

10.9 Important Notes on Using MCR Functions

Take care with blocks in which the Master Control Relay was activated with MCRA:

- If the MCR is deactivated, the value 0 is written by all assignments in program segments between ---(MCR<) and ---(MCR>).

This is valid for **all** boxes which contain an assignment, including the parameter transfer to blocks.

- The MCR is deactivated if the RLO was = 0 before an **MCR<** instruction.

Danger: PLC in STOP or undefined runtime characteristics!

The compiler also uses write access to local data behind the temporary variables defined in VAR_TEMP for calculating addresses. This means the following command sequences will set the PLC to STOP or lead to undefined runtime characteristics:

Formal parameter access

- Access to components of complex FC parameters of the type STRUCT, UDT, ARRAY, STRING
- Access to components of complex FB parameters of the type STRUCT, UDT, ARRAY, STRING from the IN_OUT area in a block with multiple instance capability (version 2 block).
- Access to parameters of a function block with multiple instance capability (version 2 block) if its address is greater than 8180.0.
- Access in a function block with multiple instance capability (version 2 block) to a parameter of the type BLOCK_DB opens DB0.

Any subsequent data access sets the CPU to STOP. T 0, C 0, FC0, or FB0 are also always used for TIMER, COUNTER, BLOCK_FC, and BLOCK_FB.

Parameter passing

- Calls in which parameters are transferred.

LAD/FBD

- T branches and midline outputs in Ladder or FBD starting with RLO = 0.

Remedy

Free the above commands from their dependence on the MCR :

- Deactivate the Master Control Relay using the **Master Control Relay**

Deactivate instruction before the statement or network in question.

- Activate the Master Control Relay again using the **Master Control Relay**

Activate instruction after the statement or network in question.

10.10 ---(MCR<) Master Control Relay On

Important Notes on Using MCR Functions

Symbol --- (MCR<)

Description

---(MCR<) (Open a Master Control Relay zone) saves the RLO in the MCR stack.

The MCR nesting stack is a LIFO stack (last in, first out) and only 8 stack entries (nesting levels) are possible. If the stack is already full, the ---(MCR<) function produces an MCR stack fault (MCRF).

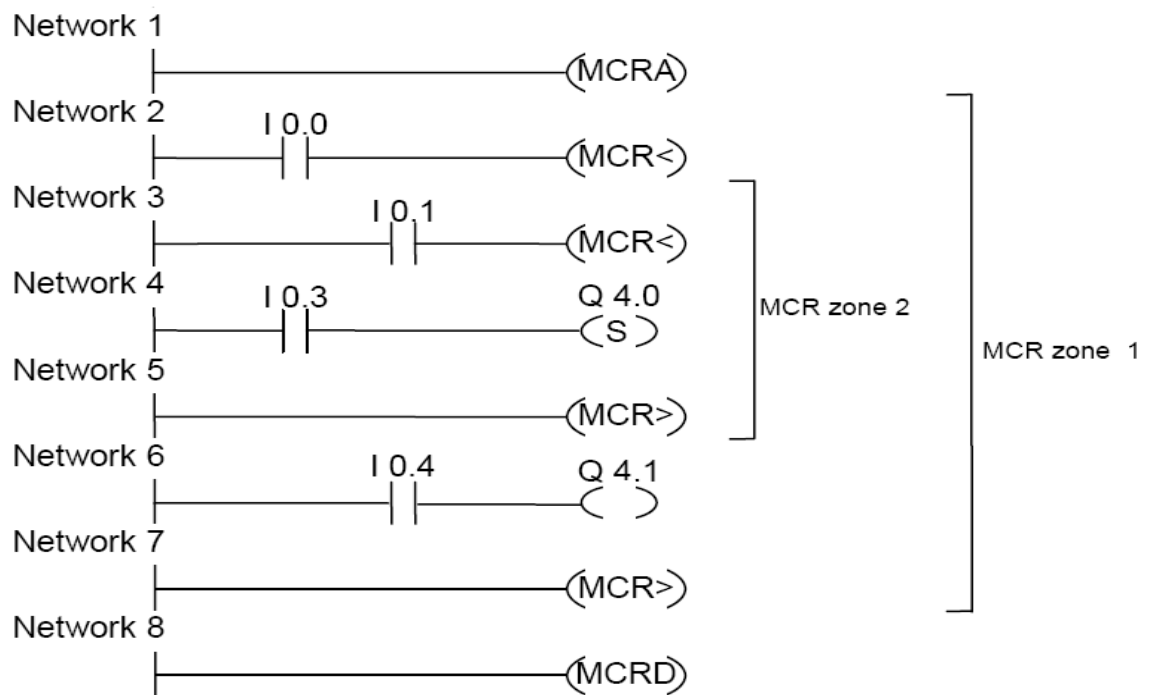
The following elements are MCR-dependent and influenced by the RLO state that is saved to the MCR stack while opening an MCR zone:

- --(#) Midline Output
- --() Output
- --(S) Set Output
- --(R) Reset Output
- RS Reset Flip Flop
- SR Set Flip Flop
- MOVE Assign a Value

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	1	-	0

Example



MCR functionality is activated by the MCRA rung.

It is then possible to create up to eight nested MCR zones. In the example there are two MCR zones.

The functions are executed as follows:

I0.0 = "1" (MCR is ON for zone 1):

the logic state of I0.4 is assigned to Q4.1

I0.0 = "0" (MCR is OFF for zone 1):

Q4.1 is "0" regardless of the logic state of I0.4

I0.1 = "1" (MCR is ON for zone 2): Q4.0 is set to "1" if I0.3 is "1"

I0.1 = "0" (MCR is OFF for zone 2): Q4.0 remains unchanged regardless the logic state of I0.3

10.11 --- (MCR>) Master Control Relay Off

Important Notes on Using MCR Functions

Symbol **---(MCR>)**

Description

---(MCR>) (close the last opened MCR zone) removes an RLO entry from the MCR stack.

The MCR nesting stack is a LIFO stack (last in, first out) and only 8 stack entries (nesting levels) are possible.

If the stack is already empty, ---(MCR>) produces an MCR stack fault (MCRF).

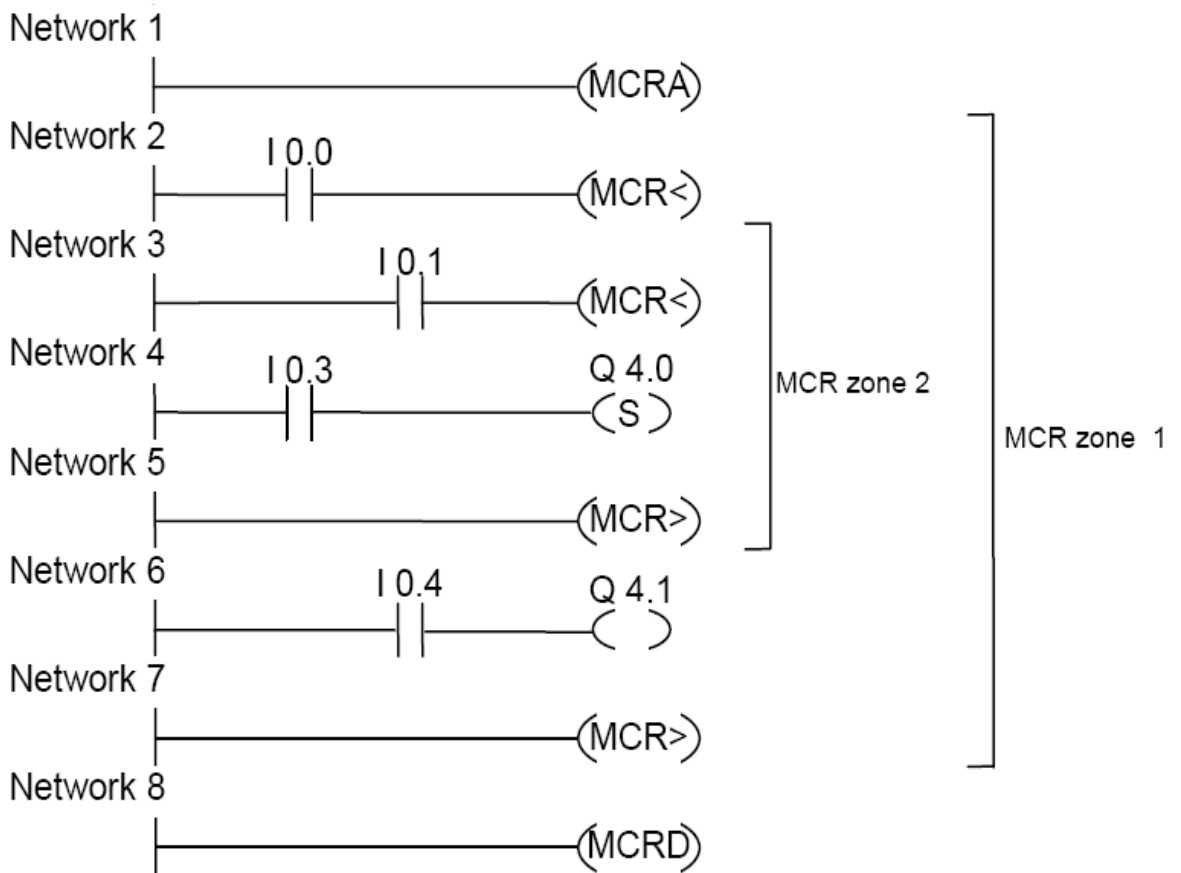
The following elements are MCR-dependent and influenced by the RLO state that is saved to the MCR stack while opening the MCR zone:

- --(#) Midline Output
- --() Output
- --(S) Set Output
- --(R) Reset Output
- RS Reset Flip Flop
- SR Set Flip Flop
- MOVE Assign a Value

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	1	-	0

Example



MCR functionality is activated by the ---(MCRA) rung.

It is then possible to create up to eight nested MCR zones.

In the example there are two MCR zones.

The first ---(MCR>) (MCR OFF) rung belongs to the second

---(MCR<) (MCR ON) rung.

All rungs between belong to the MCR zone 2. The functions are executed as follows:

I0.0 = "1": the logic state of I0.4 is assigned to Q4.1

I0.0 = "0": Q4.1 is "0" regardless of the logic state of I0.4

I0.1 = "1": Q4.0 is set to "1" if I0.3 is "1"

I0.1 = "0": Q4.0 remains unchanged regardless of the logic state of I0.3

10.12 ---(MCRA) Master Control Relay Activate

Important Notes on Using MCR Functions

Symbol

---(MCRA)

Description

---(MCRA) (Activate Master Control Relay) activates master control relay function.

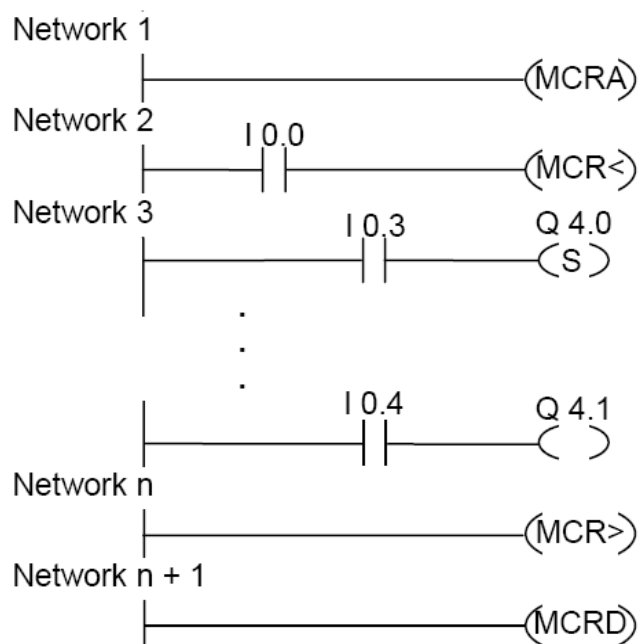
After this command, it is possible to program MCR zones with the commands:

- ---(MCR<)
- ---(MCR>)

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	-	-	-	-

Example



MCR functionality is activated by the MCRA rung.

The rungs between the MCR< and the MCR> (outputs Q4.0, Q4.1) are executed as follows:

I0.0 = "1" (MCR is ON):

Q4.0 is set to "1" if I0.3 is logic "1", or will remain unchanged if I0.3 is "0" and the logic state of I0.4 is assigned to Q4.1

I0.0 = "0" (MCR is OFF):

Q4.0 remains unchanged regardless of the logic state of I0.3 and Q4.1 is "0" regardless of the logic state of I0.4

In the next rung, the instruction ---(MCRD) deactivates the MCR.

This means that you cannot program any more MCR zones using the instruction pair ---(MCR<) and ---(MCR>).

10.13 ---(MCRD) Master Control Relay Deactivate

Important Notes on Using MCR Functions

Symbol

---(MCRD)

Description

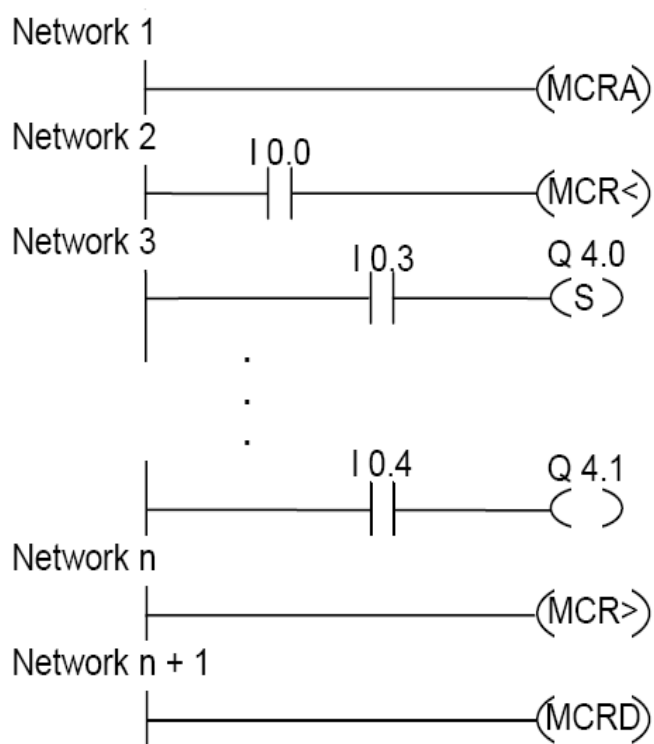
---(MCRD) (Deactivate Master Control Relay) deactivates MCR functionality.

After this command, you cannot program MCR zones.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	-	-	-	-

Example



MCR functionality is activated by the MCRA rung.

The rungs between the MCR< and the MCR> (outputs Q4.0, Q4.1) are executed as follows:

I0.0 = "1" (MCR is ON):

Q4.0 is set to "1" if I0.3 is logic "1" and the logic state of I0.4 is assigned to Q4.1.

I0.0 = "0" (MCR is OFF):

Q4.0 remains unchanged regardless of the logic state of I0.3 and Q4.1 is "0" regardless of the logic state of I0.4.

In the next rung, the instruction ---(MCRD) deactivates the MCR.

This means that you cannot program any more MCR zones using the instruction pair ---(MCR<) and ---(MCR>).

10.14 ---(RET) Return

Symbol

---(RET)

Description

RET (Return) is used to conditionally exit blocks. For this output, a preceding logic operation is required.

Status word

Conditional Return (Return if RLO = "1"):

Status word

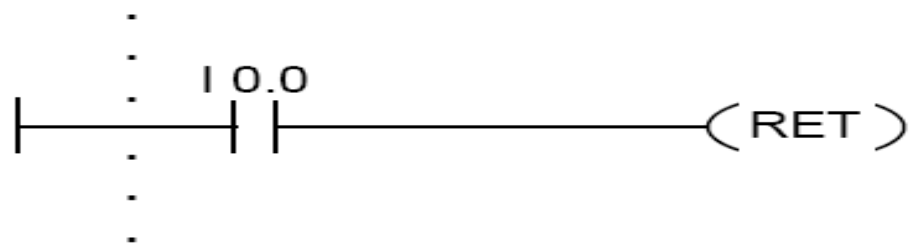
Conditional Return (Return if RLO = "1"):

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	*	-	-	-	0	0	1	1	0

The operation **RET** is shown internally in the sequence "SAVE; BEC, ".

This also affects the BR bit.

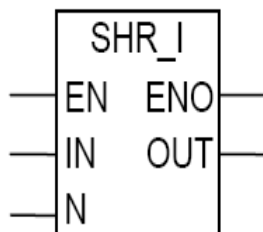
Example



The block is exited if I0.0 is "1".

11.1.2 SHR_I Shift Right Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	INT	I, Q, M, L, D	Value to shift
N	WORD	I, Q, M, L, D	Number of bit positions to shift
OUT	INT	I, Q, M, L, D	Result of shift instruction

Description

SHR_I (Shift Right Integer) is activated by a logic "1" at the Enable (EN) Input.

The SHR_I instruction is used to shift bits 0 to 15 of input IN bit by bit to the right.

Bits 16 to 31 are not affected.

The input N specifies the number of bits by which to shift.

If N is larger than 16, the command acts as if N were equal to 16.

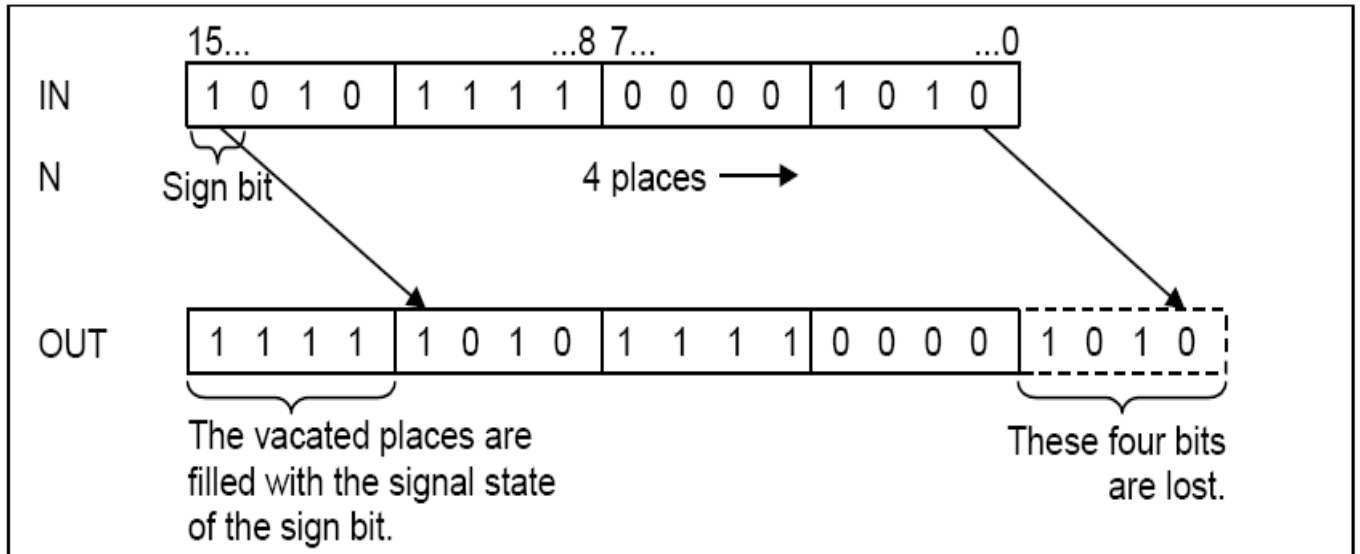
The bit positions shifted in from the left to fill vacated bit positions are assigned the logic state of bit 15 (sign bit for the integer).

This means these bit positions are assigned "0" if the integer is positive and "1" if the integer is negative.

The result of the shift instruction can be scanned at output OUT.

The CC 0 bit and the OV bit are set to "0" by SHR_I if N is not equal to 0.

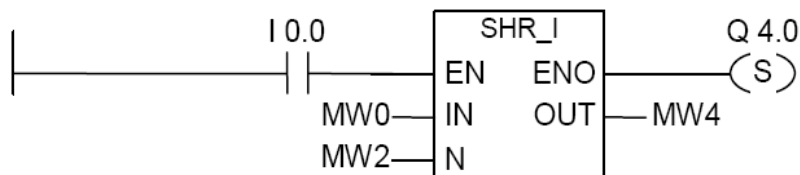
ENO has the same signal state as EN.



Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	-	x	x	x	1

Example



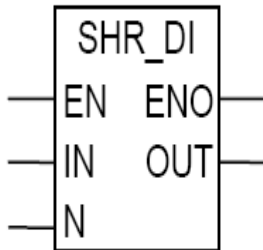
The SHR_I box is activated by logic "1" at I0.0.

MW0 is loaded and shifted right by the number of bits specified with MW2.

The result is written to MW4. Q4.0 is set.

11.1.3 SHR_DI Shift Right Double Integer

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	DINT	I, Q, M, L, D	Value to shift
N	WORD	I, Q, M, L, D	Number of bit positions to shift
OUT	DINT	I, Q, M, L, D	Result of shift instruction

Description

SHR_DI (Shift Right Double Integer) is activated by a logic "1" at the Enable (EN) Input.

The SHR_DI instruction is used to shift bits 0 to 31 of input IN bit by bit to the right.

The input N specifies the number of bits by which to shift. If N is larger than 32, the command acts as if N were equal to 32.

The bit positions shifted in from the left to fill vacated bit positions are assigned the logic state of bit 31 (sign bit for the double integer).

This means these bit positions are assigned "0" if the integer is positive and "1" if the integer is negative.

The result of the shift instruction can be scanned at output OUT.

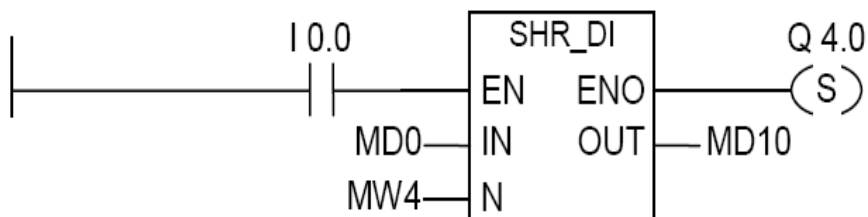
The CC 0 bit and the OV bit are set to "0" by SHR_DI if N is not equal to 0.

ENO has the same signal state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	-	x	x	x	1

Example



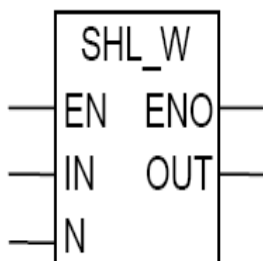
The SHR_DI box is activated by logic "1" at I0.0.

MD0 is loaded and shifted right by the number of bits specified with MW4.

The result is written to MD10. Q4.0 is set.

11.1.4 SHL_W Shift Left Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	WORD	I, Q, M, L, D	Value to shift
N	WORD	I, Q, M, L, D	Number of bit positions to shift
OUT	WORD	I, Q, M, L, D	Result of shift instruction

Description

SHL_W (Shift Left Word) is activated by a logic "1" at the Enable (EN) Input.

The SHL_W instruction is used to shift bits 0 to 15 of input IN bit by bit to the left.

Bits 16 to 31 are not affected.

The input N specifies the number of bits by which to shift.

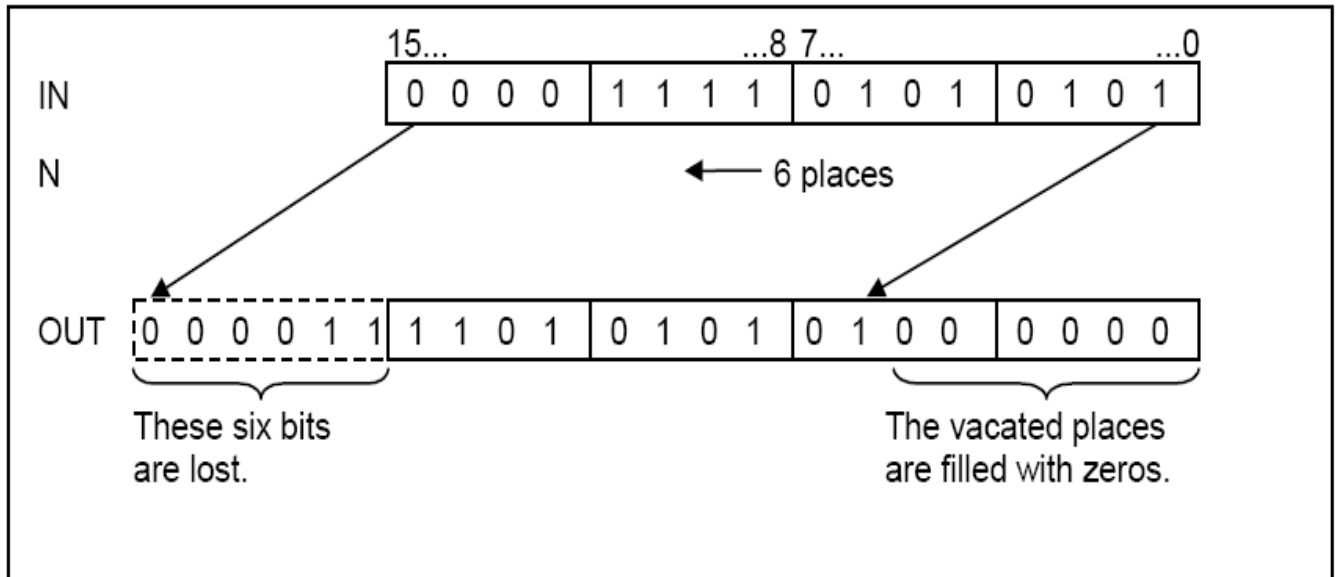
If N is larger than 16, the command writes a "0" at output OUT and sets the bits CC 0 and OV in the status word to "0".

N zeros are also shifted in from the right to fill vacated bit positions.

The result of the shift instruction can be scanned at output OUT.

The CC 0 bit and the OV bit are set to "0" by SHL_W if N is not equal to 0.

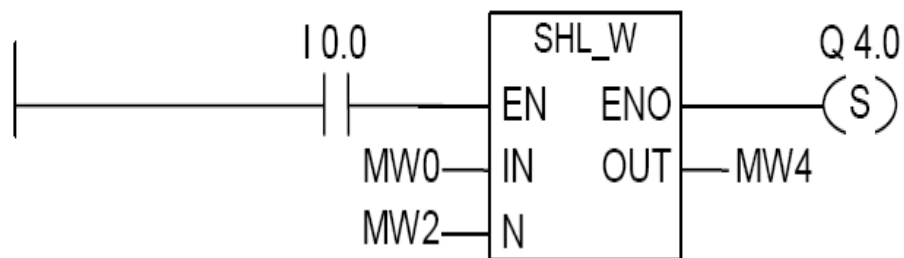
ENO has the same signal state as EN.



Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	-	X	X	X	1

Example

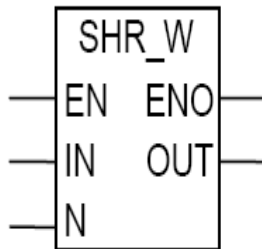


The SHL_W box is activated by logic "1" at I0.0. MW0 is loaded and shifted left by the number of bits specified with MW2.

The result is written to MW4. Q4.0 is set.

11.1.5 SHR_W Shift Right Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	WORD	I, Q, M, L, D	Value to shift
N	WORD	I, Q, M, L, D	Number of bit positions to shift
OUT	WORD	I, Q, M, L, D	Result word of shift instruction

Description

SHR_W (Shift Right Word) is activated by a logic "1" at the Enable (EN) Input.

The SHR_W instruction is used to shift bits 0 to 15 of input IN bit by bit to the right.

Bits 16 to 31 are not affected. The input N specifies the number of bits by which to shift.

If N is larger than 16, the command writes a "0" at output OUT and sets the bits CC 0 and OV in the status word to "0".

N zeros are also shifted in from the left to fill vacated bit positions.

The result of the shift instruction can be scanned at output OUT.

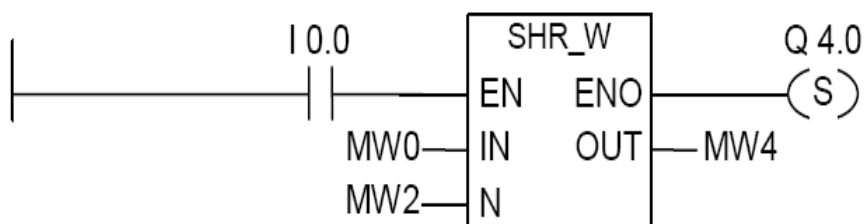
The CC 0 bit and the OV bit are set to "0" by SHR_W if N is not equal to 0.

ENO has the same signal state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	-	x	x	x	1

Example



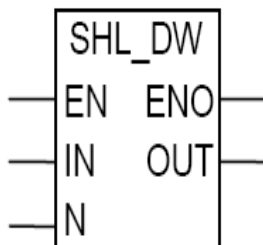
The SHR_W box is activated by logic "1" at I0.0.

MW0 is loaded and shifted right by the number of bits specified with MW2.

The result is written to MW4. Q4.0 is set.

11.1.6 SHL_DW Shift Left Double Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	DWORD	I, Q, M, L, D	Value to shift
N	WORD	I, Q, M, L, D	Number of bit positions to shift
OUT	DWORD	I, Q, M, L, D	Result double word of shift instruction

Description

SHL_DW (Shift Left Double Word) is activated by a logic "1" at the Enable (EN) Input.

The SHL_DW instruction is used to shift bits 0 to 31 of input IN bit by bit to the left.

The input N specifies the number of bits by which to shift.

If N is larger than 32, the command writes a "0" at output OUT and sets the bits CC 0 and OV in the status word to "0".

N zeros are also shifted in from the right to fill vacated bit positions.

The result double word of the shift instruction can be scanned at output OUT.

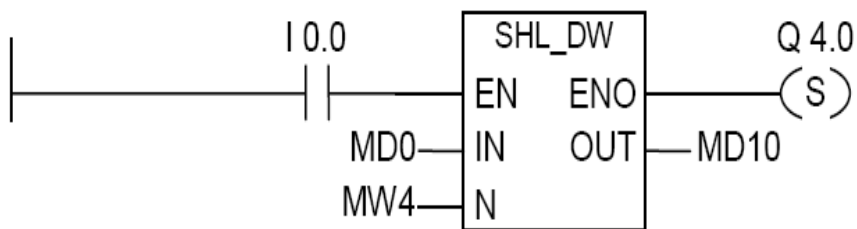
The CC 0 bit and the OV bit are set to "0" by SHL_DW if N is not equal to 0.

ENO has the same signal state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	-	x	x	x	1

Example



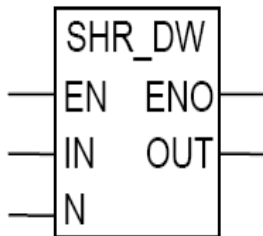
The SHL_DW box is activated by logic "1" at I0.0.

MD0 is loaded and shifted left by the number of bits specified with MW4.

The result is written to MD10. Q4.0 is set.

11.1.7 SHR_DW Shift Right Double Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	DWORD	I, Q, M, L, D	Value to shift
N	WORD	I, Q, M, L, D	Number of bit positions to shift
OUT	DWORD	I, Q, M, L, D	Result double word of shift instruction

Description

SHR_DW (Shift Right Double Word) is activated by a logic "1" at the Enable (EN) Input.

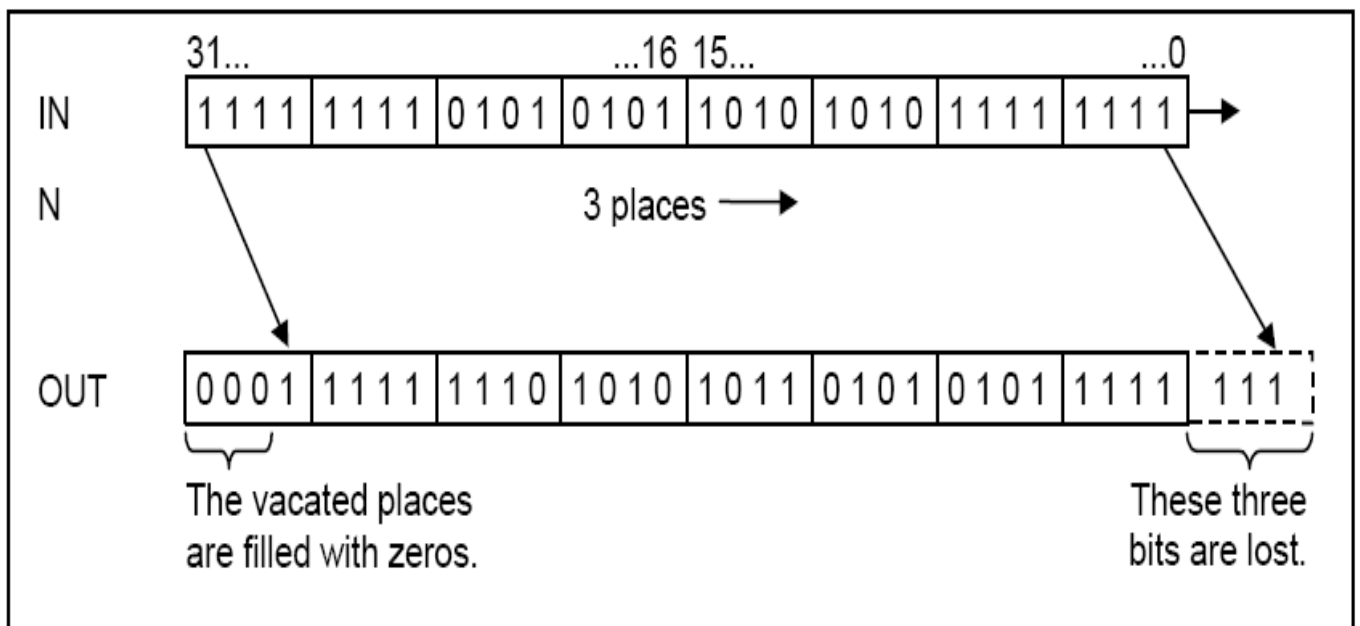
The SHR_DW instruction is used to shift bits 0 to 31 of input IN bit by bit to the right. The input N specifies the number of bits by which to shift. If N is larger than 32, the command writes a "0" at output OUT and sets the bits CC 0 and OV in the status word to "0".

N zeros are also shifted in from the left to fill vacated bit positions.

The result double word of the shift instruction can be scanned at output OUT.

The CC 0 bit and the OV bit are set to "0" by SHR_DW if N is not equal to 0.

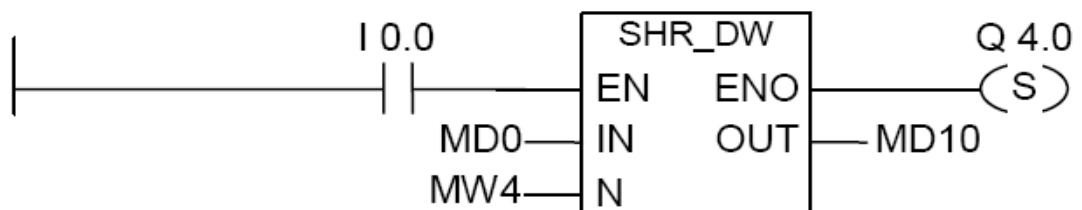
ENO has the same signal state as EN.



Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	X	X	X	X	-	X	X	X	1

Example



The SHR_DW box is activated by logic "1" at I0.0.

MD0 is loaded and shifted right by the number of bits specified with MW4.

The result is written to MD10. Q4.0 is set.

11.2 Rotate Instructions

11.2.1 Overview of Rotate Instructions

Description

You can use the Rotate instructions to rotate the entire contents of input IN bit by bit to the left or to the right.

The vacated bit places are filled with the signal states of the bits that are shifted out of input IN.

The number that you supply for input parameter N specifies the number of bits by which to rotate.

Depending on the instruction, rotation takes place via the CC 1 bit of the status word.

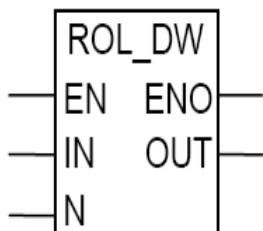
The CC 0 bit of the status word is reset to 0.

The following rotate instructions are available:

- ROL_DW Rotate Left Double Word
- ROR_DW Rotate Right Double Word

11.2.2 ROL_DW Rotate Left Double Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	DWORD	I, Q, M, L, D	Value to rotate
N	WORD	I, Q, M, L, D	Number of bit positions to rotate
OUT	DWORD	I, Q, M, L, D	Result double word of rotate instruction

Description

ROL_DW (Rotate Left Double Word) is activated by a logic "1" at the Enable (EN) Input.

The ROL_DW instruction is used to rotate the entire contents of input IN bit by bit to the left. The input N specifies the number of bits by which to rotate.

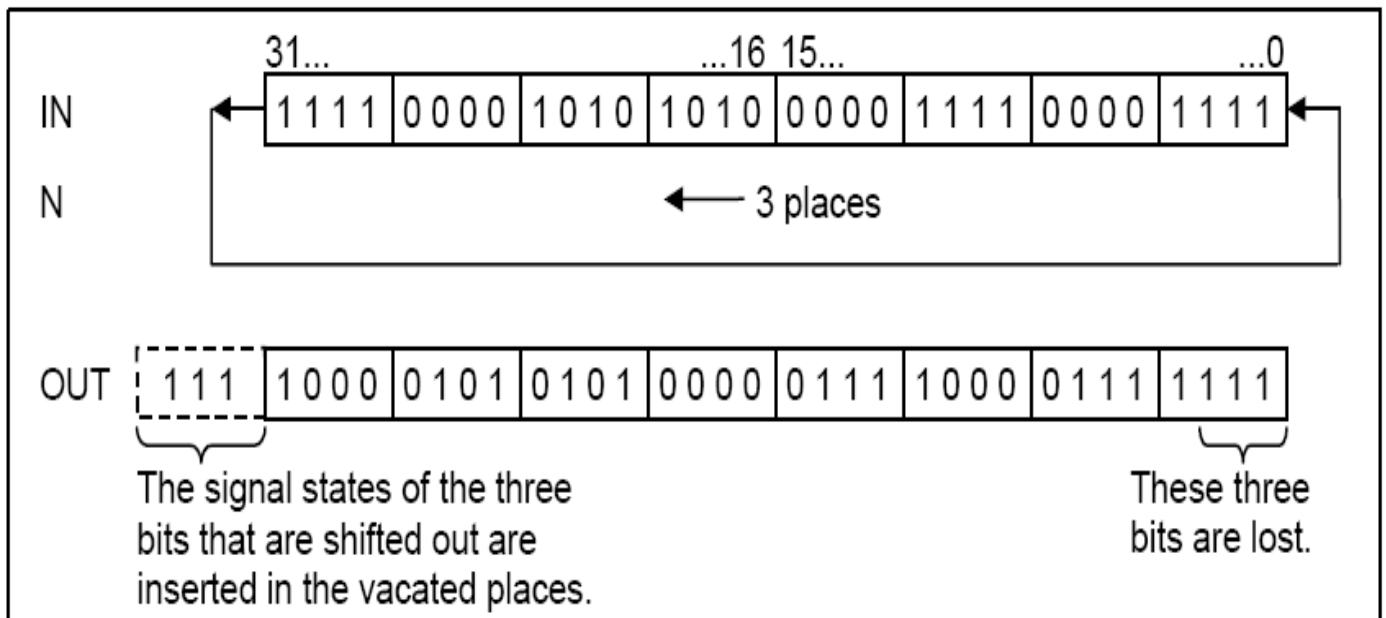
If N is larger than 32, the double word IN is rotated by $((N-1) \text{ modulo } 32)+1$ positions.

The bit positions shifted in from the right are assigned the logic states of the bits which were rotated out to the left.

The result double word of the rotate instruction can be scanned at output OUT.

The CC 0 bit and the OV bit are set to "0" by ROL_DW if N is not equal to 0.

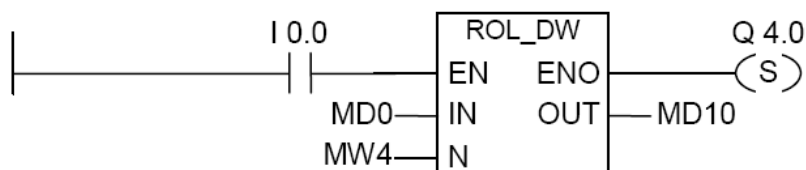
ENO has the same signal state as EN.



Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	-	x	x	x	1

Example



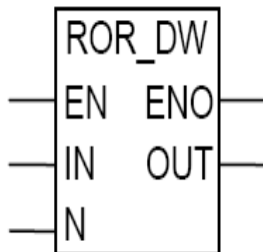
The ROL_DW box is activated by logic "1" at I0.0.

MD0 is loaded and rotated to the left by the number of bits specified with MW4.

The result is written to MD10. Q4.0 is set.

11.2.3 ROR_DW Rotate Right Double Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN	DWORD	I, Q, M, L, D	Value to rotate
N	WORD	I, Q, M, L, D	Number of bit positions to rotate
OUT	DWORD	I, Q, M, L, D	Result double word of rotate instruction

Description

ROR_DW (Rotate Right Double Word) is activated by a logic "1" at the Enable (EN) Input. The ROR_DW instruction is used to rotate the entire contents of input IN bit by bit to the right.

The input N specifies the number of bits by which to rotate.

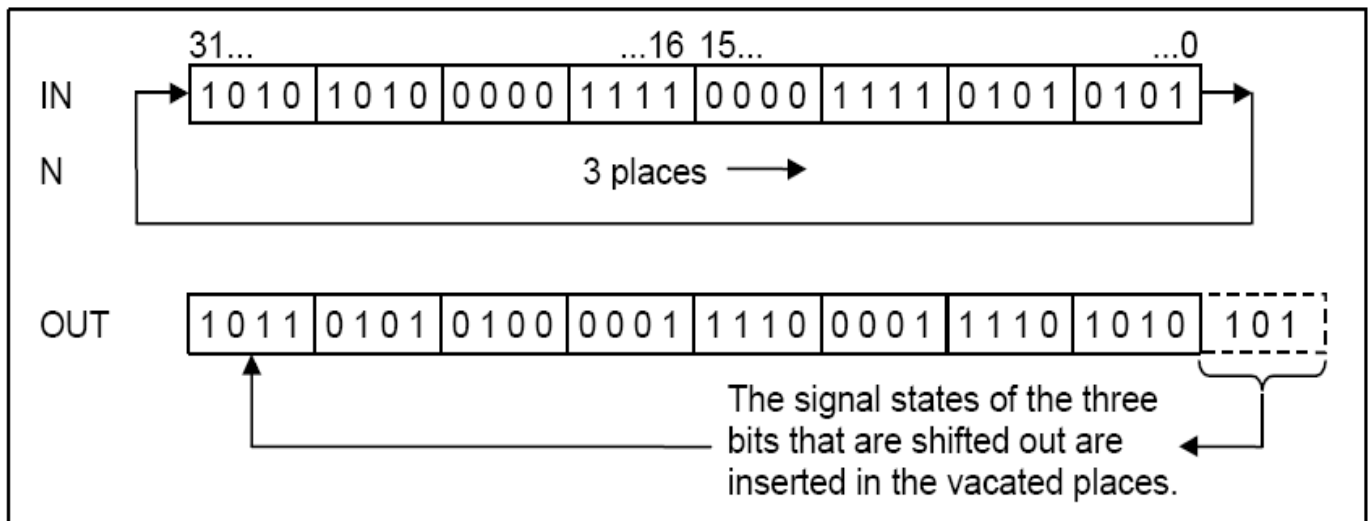
If N is larger than 32, the double word IN is rotated by $((N-1) \text{ modulo } 32)+1$ positions.

The bit positions shifted in from the left are assigned the logic states of the bits which were rotated out to the right.

The result double word of the rotate instruction can be scanned at output OUT.

The CC 0 bit and the OV bit are set to "0" by ROR_DW if N is not equal to 0.

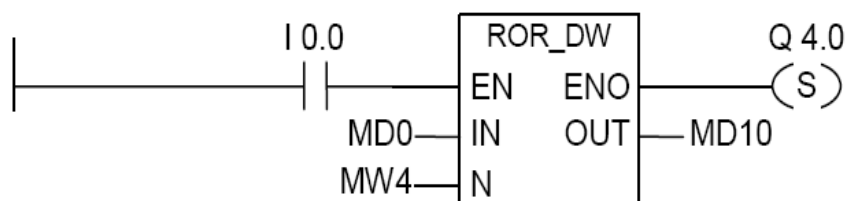
ENO has the same signal state as EN.



Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	x	x	x	x	-	x	x	x	1

Example



The ROR_DW box is activated by logic "1" at I0.0.

MD0 is loaded and rotated to the right by the number of bits specified with MW4.

The result is written to MD10. Q4.0 is set.

12.1 Overview of Statusbit Instructions

Description

The status bit instructions are bit logic instructions that work with the bits of the status word.

Each of these instructions reacts to one of the following conditions that is indicated by one or more bits of the status word:

- The Binary Result bit (BR ---I I---) is set (that is, has a signal state of 1).
- A math function had an Overflow (OV ---I I---)
or a Stored Overflow (OS ---I I---).
- The result of a math function is unordered (UO ---I I---).
- The result of a math function is related to 0 in one of the following ways:
== 0, <> 0, > 0, < 0, >= 0, <= 0.

When a status bit instruction is connected in series, it combines the result of its signal state check with the previous result of logic operation according to the And truth table.

When a status bit instruction is connected in parallel, it combines its result with the previous RLO according to the Or truth table.

12.2 OV ---| |--- Exception Bit Overflow

Symbol



Description

OV ---| |--- (Exception Bit Overflow) or **OV ---| / |---** (Negated Exception Bit Overflow) contact symbols are used to recognize an overflow in the last math function executed.

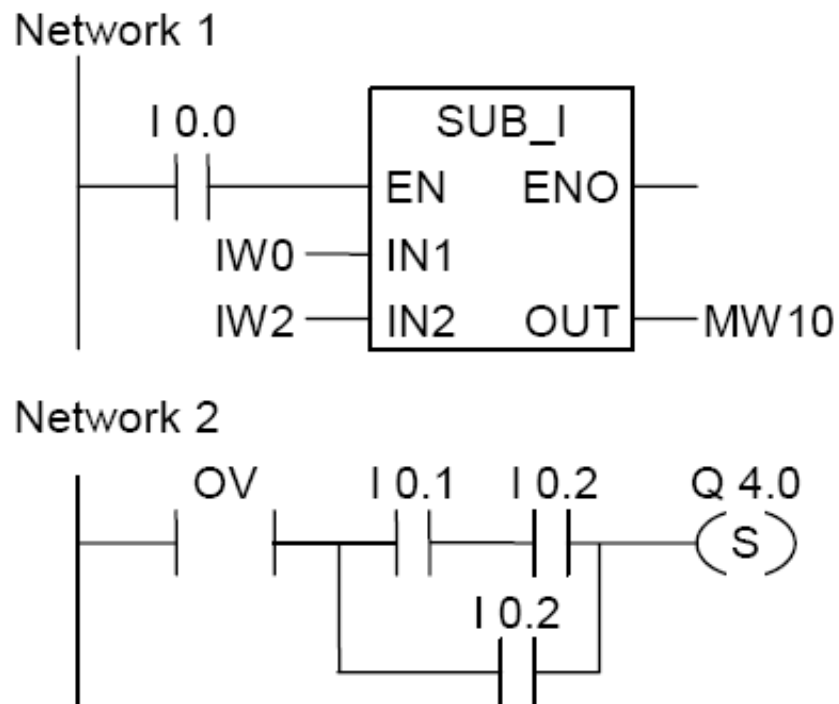
This means that after the function executes, the result of the instruction is outside the permissible negative or positive range.

Used in series, the result of the scan is linked to the RLO by AND, used in parallel, it is linked to the RLO by OR.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



The box is activated by signal state "1" at I0.0.

If the result of the math function "IW0 - IW2" is outside the permissible range for an integer, the OV bit is set.

The signal state scan at OV is "1". Q4.0 is set if the scan of OV is signal state "1" and the RLO of network 2 is "1".

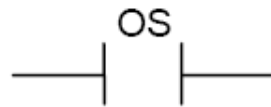
Note

The scan with OV is only necessary because of the two separate networks.

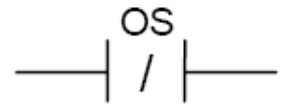
Otherwise it is possible to take the ENO output of the math function that is "0" if the result is outside the permissible range.

12.3 OS ---| |--- Exception Bit Overflow Stored

Symbol



or negation



Description

OS ---| |--- (Exception Bit Overflow Stored) or **OS ---| / |---** (Negated Exception Bit Overflow Stored) contact symbols are used to recognize and store a latching overflow in a math function. If the result of the instruction lies outside the permissible negative or positive range, the OS bit in the status word is set. Unlike the OV bit, which is rewritten for subsequent math functions, the OS bit stores an overflow when it occurs.

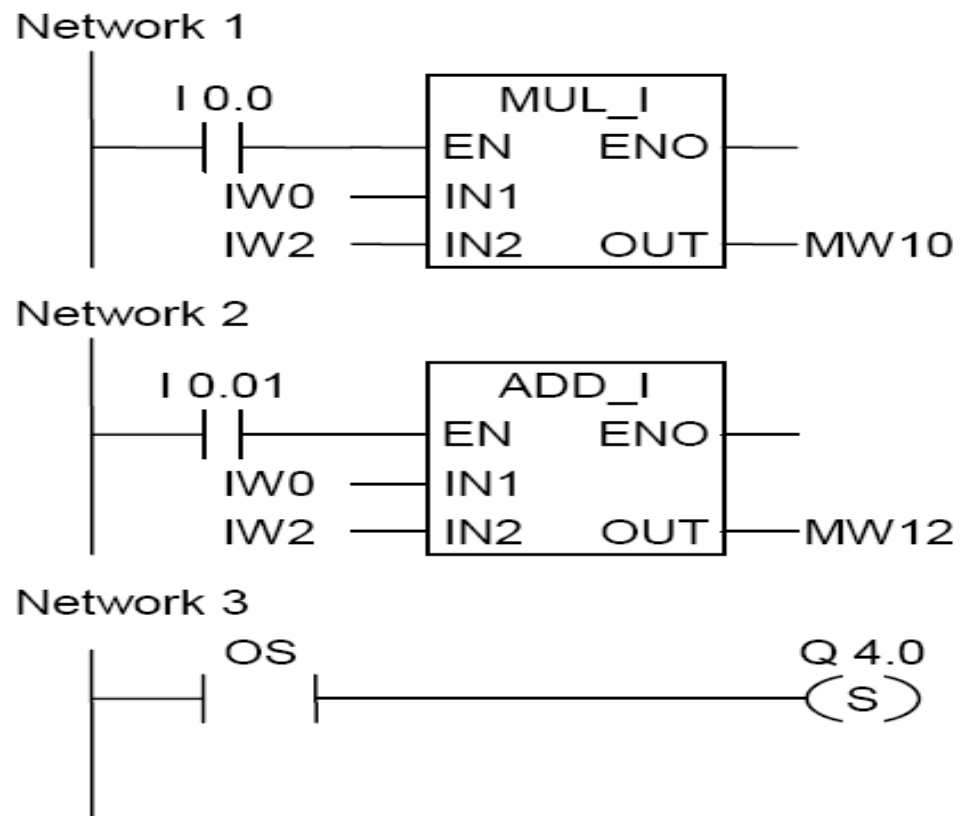
The OS bit remains set until the block is left.

Used in series, the result of the scan is linked to the RLO by AND, used in parallel, it is linked to the RLO by OR.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



The `MUL_I` box is activated by signal state "1" at `I0.0`.

The `ADD_I` box is activated by logic "1" at `I0.1`.

If the result of one of the math functions was outside the permissible range for an integer, the `OS` bit in the status word is set to "1".

`Q4.0` is set if the scan of `OS` is logic "1".

Note

The scan with `OS` is only necessary because of the two separate networks.

Otherwise it is possible to take the `ENO` output of the first math function and connect it with the `EN` input of the second (cascade arrangement).

12.4 UO ---| |--- Exception Bit Unordered

Symbol



Description

UO ---| |--- (Exception Bit Unordered) or **UO ---| / |---** (Negated Exception Bit Unordered) contact symbols are used to recognize if the math function with floating-point numbers is unordered (meaning, whether one of the values in the math function is an invalid floating-point number).

If the result of a math function with floating-point numbers (UO) is invalid, the signal state scan is "1".

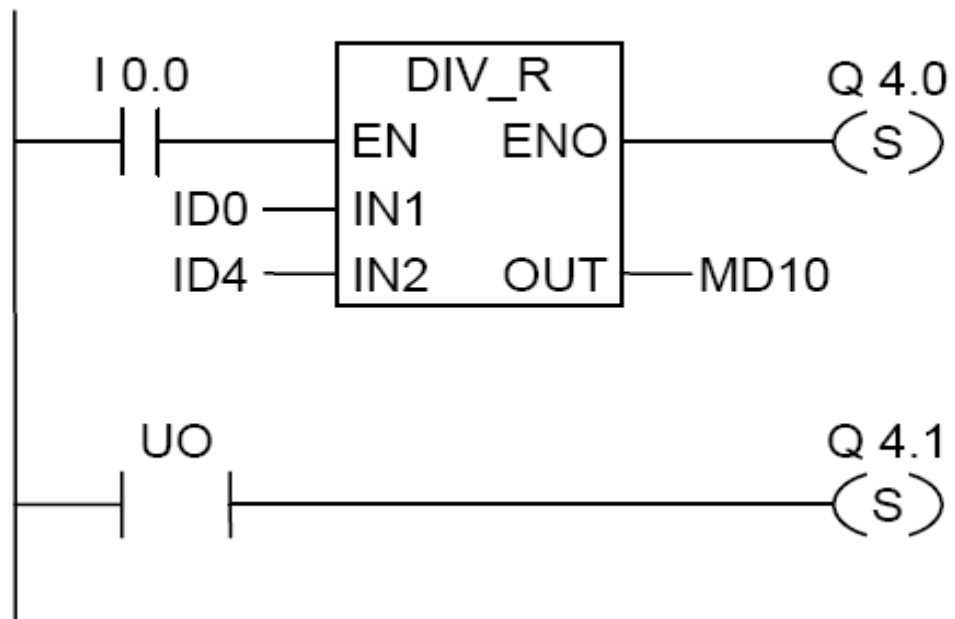
If the logic operation in CC 1 and CC 0 shows "not invalid", the result of the signal state scan is "0".

Used in series, the result of the scan is linked to the RLO by AND, used in parallel it is linked to the RLO by OR.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



The box is activated by signal state "1" at I0.0.

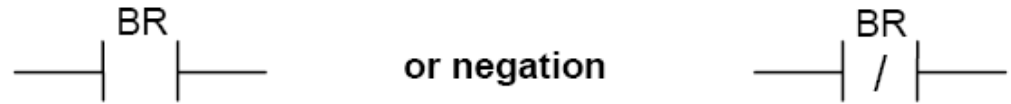
If the value of ID0 or ID4 is an invalid floating-point number, the math function is invalid.

If the signal state of EN = 1 (activated) and if an error occurs during the processing of the function DIV_R, the signal state of ENO = 0.

Output Q4.1 is set when the function DIV_R is executed but one of the values is not a valid **floating-point number**.

12.5 BR ---| |--- Exception Bit Binary Result

Symbol



Description

BR ---| |--- (Exception Bit BR Memory) or **BR ---| / |---** (Negated Exception Bit BR Memory) contact symbols are used to test the logic state of the BR bit in the status word.

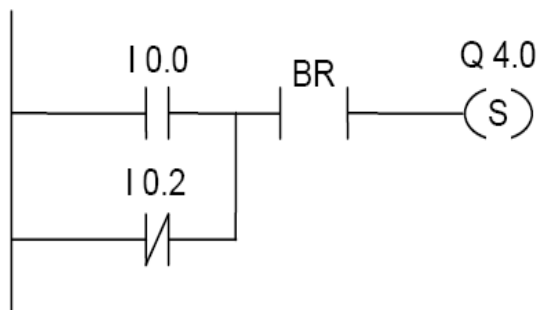
Used in series, the result of the scan is linked to the RLO by AND, used in parallel, it is linked to the RLO by OR.

The BR bit is used in the transition from word to bit processing.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	x	x	x	1

Example



Q4.0 is set if I0.0 is "1" or I0.2 is "0" and in addition to this RLO the logic state of the BR bit is "1".

12.6 ==0 ---| |--- Result Bit Equal 0

Symbol



Description

==0 ---| |--- (Result Bit Equal 0) or ==0 ---| / |--- (Negated Result Bit Equal 0)

contact symbols are used to recognize if the result of a math function is equal to "0".

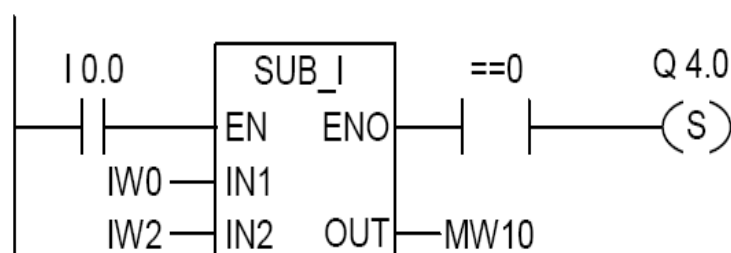
The instructions scan the condition code bits CC 1 and CC 0 in the status word in order to determine the relation of the result to "0".

Used in series, the result of the scan is linked to the RLO by AND, used in parallel, it is linked to the RLO by OR.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	x	x	x	1

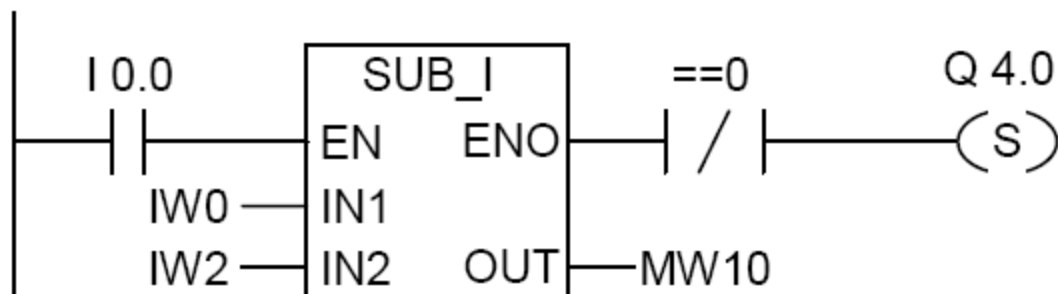
Examples



The box is activated by signal state "1" at I0.0.

If the value of IW0 is equal to the value of IW2, the result of the math function "IW0 - IW2" is "0".

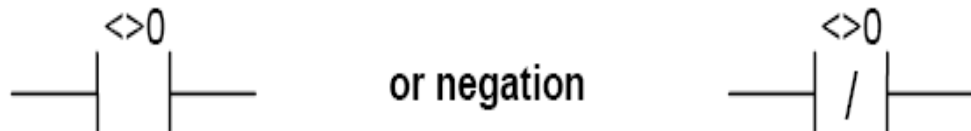
Q4.0 is set if the function is properly executed and the result is **equal** to "0".



Q4.0 is set if the function is properly executed and the result is **not equal** to "0".

12.7 <>0 ---| |--- Result Bit Not Equal 0

Symbol



Description

<>0 ---| |--- (Result Bit Not Equal 0)

or <>0 ---| / |--- (Negated Result Bit Not Equal 0) contact symbols are used to recognize if the result of a math function is not equal to "0".

The instructions scan the condition code bits CC 1 and CC 0 in

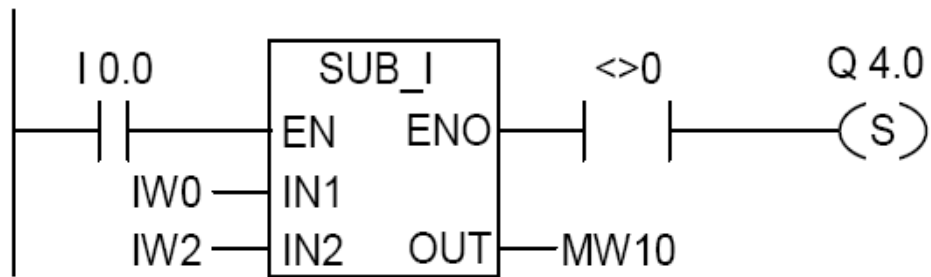
The status word in order to determine the relation of the result to "0".

Used in series, the result of the scan is linked to the RLO by AND, used in parallel, it is linked to the RLO by OR.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

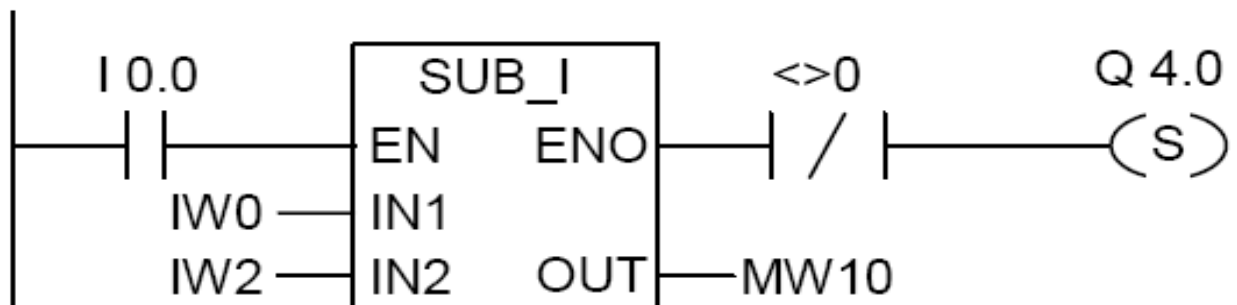
Examples



The box is activated by signal state "1" at I0.0.

If the value of IW0 is different to the value of IW2, the result of the math function "IW0 - IW2" is not equal to "0".

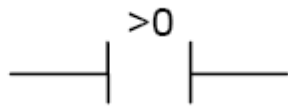
Q4.0 is set if the function is properly executed and the result is **not equal** to "0".



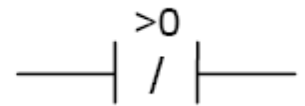
Q4.0 is set if the function is properly executed and the result is **equal** to "0".

12.8 >0 ---| |--- Result Bit Greater Than 0

Symbol



or negation



Description

>0 ---| |--- (Result Bit Greater Than 0)

or >0 ---| / |--- (Negated Result Bit Greater

Than Zero) contact symbols are used to recognize if the result of a math function is greater than "0".

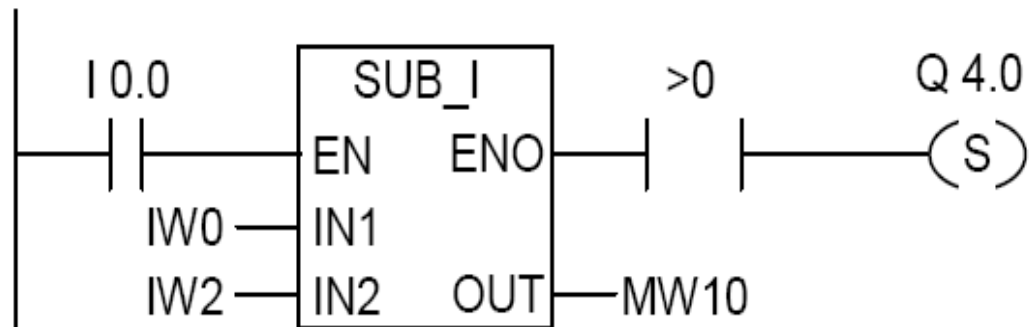
The instructions scan the condition code bits CC 1 and CC 0 in the status word in order to determine the relation to "0".

Used in series, the result of the scan is linked to the RLO by AND, used in parallel, it is linked to the RLO by OR.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

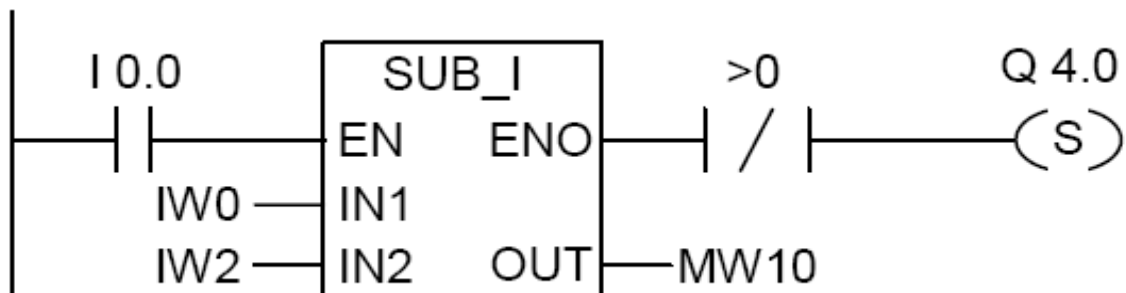
Example



The box is activated by signal state "1" at I0.0.

If the value of IW0 is higher than the value of IW2, the result of the math function "IW0 - IW2" is greater than "0".

Q4.0 is set if the function is properly executed and the result is **greater** than "0".



Q4.0 is set if the function is properly executed and the result is **not** greater than "0".

12.9 <0 ---| |--- Result Bit Less Than 0

Symbol



Description

<0 ---| |--- (Result Bit Less Than 0)

or <0 ---| / |--- (Negated Result Bit Less Than 0) contact symbols are used to recognize if the result of a math function is less than "0".

The instructions scan the condition code bits CC 1 and CC 0 in

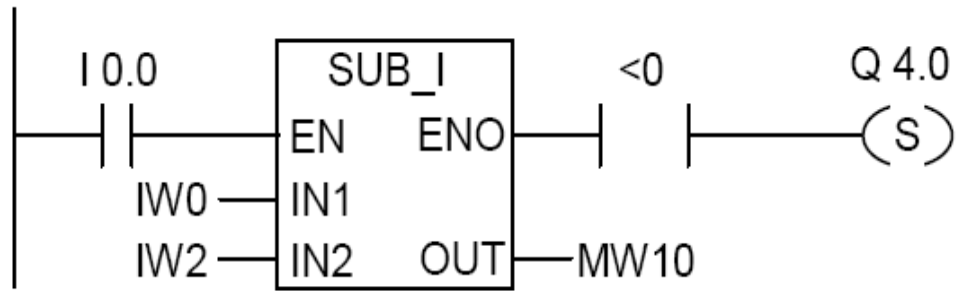
The status word in order to determine the relation of the result to "0".

Used in series, the result of the scan is linked to the RLO by AND, used in parallel, it is linked to the RLO by OR.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

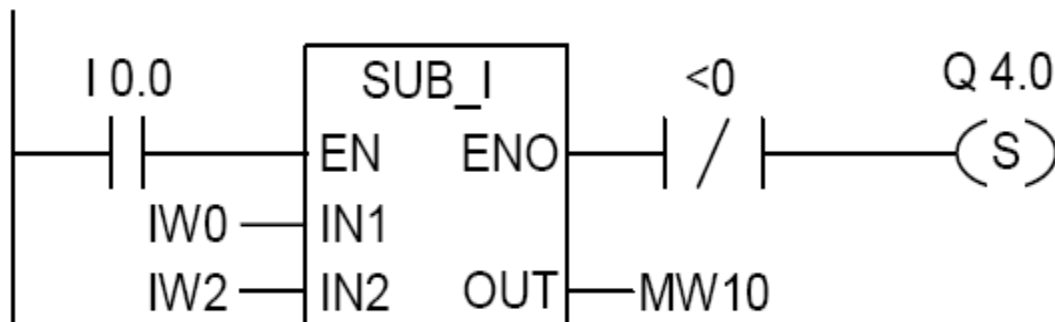
Example



The box is activated by signal state "1" at I0.0.

If the value of IW0 is lower than the value of IW2, the result of the math function "IW0 - IW2" is less than "0".

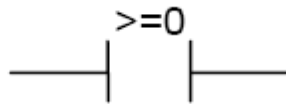
Q4.0 is set if the function is properly executed and the result is **less** than "0".



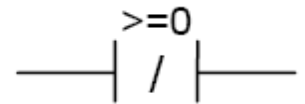
Q4.0 is set if the function is properly executed and the result is **not** less than "0".

12.10 ≥ 0 ---| |--- Result Bit Greater Equal 0

Symbol



or negation



Description

≥ 0 ---| |--- (Result Bit Greater Equal 0)

or ≥ 0 ---| / |--- (Negated Result Bit

Greater Equal 0) contact symbols are used to recognize if the result of a math function is greater than or equal to "0".

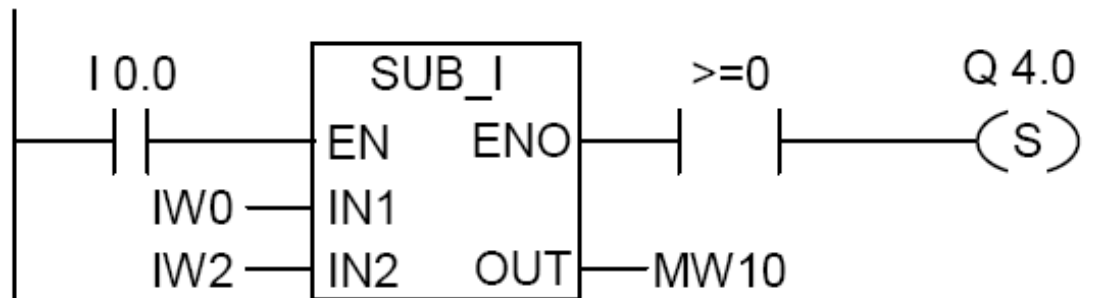
The instructions scan the condition code bits CC 1 and CC 0 in the status word in order to determine the relation to "0".

Used in series, the result of the scan is linked to the RLO by AND, used in parallel, it is linked to the RLO by OR.

Status word

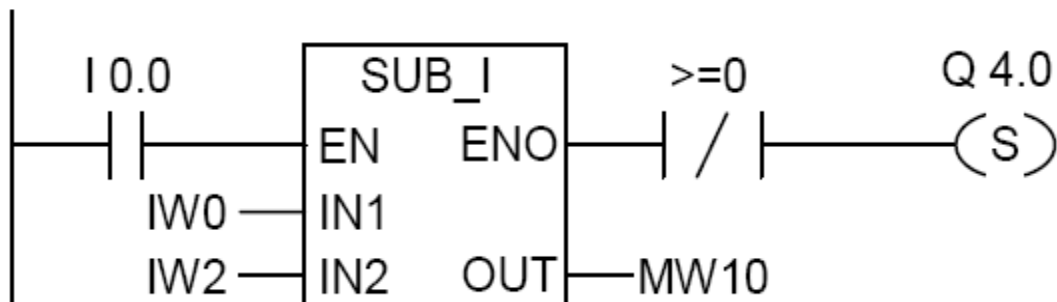
	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



The box is activated by signal state "1" at I0.0. If the value of IW0 is higher or equal to the value of IW2, the result of the math function "IW0 - IW2" is greater than or equal to "0".

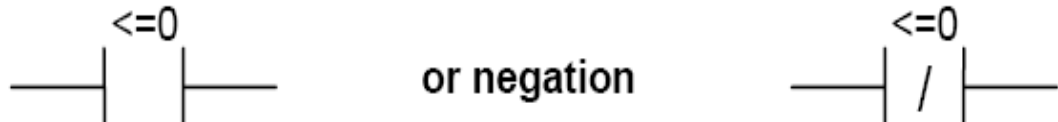
Q4.0 is set if the function is properly executed and the result is **greater** than or equal to "0".



Q4.0 is set if the function is properly executed and the result is **not** greater than or equal to "0".

12.11 <=0 ---| |--- Result Bit Less Equal 0

Symbol



Description

<=0 ---| |--- (Result Bit Less Equal 0)

or <=0 ---| / |--- (Negated Result Bit Less

Equal 0) contact symbols are used to recognize if the result of a math function is less than or equal to "0".

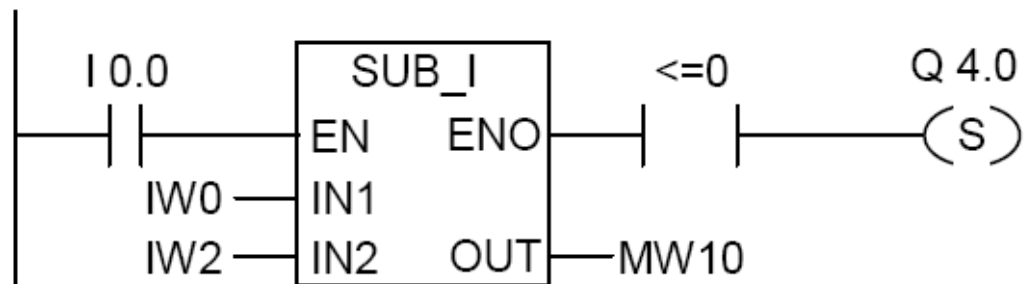
The instructions scan the condition code bits CC 1 and CC 0 in the status word in order to determine the relation of the result to "0".

Used in series, the result of the scan is linked to the RLO by AND, used in parallel, it is linked to the RLO by OR.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Examples



The box is activated by signal state "1" at I0.0.

If the value of IW0 is less than or equal to the value of IW2 the result of the math function "IW0 - IW2" is less than or equal to "0".

Q4.0 is set if the function is well properly executed and the result is **less** than or equal to "0".

13 Timer Instructions

13.1 Overview of Timer Instructions

Description

You can find information for setting and selecting the correct time under "Location of a Timer in Memory and Components of a Timer".

The following timer instructions are available:

- S_PULSE Pulse S5 Timer
- S_PEXT Extended Pulse S5 Timer
- S_ODT On-Delay S5 Timer
- S_ODTS Retentive On-Delay S5 Timer
- S_OFFDT Off-Delay S5 Timer
- ---(SP) Pulse Timer Coil
- ---(SE) Extended Pulse Timer Coil
- ---(SD) On-Delay Timer Coil
- ---(SS) Retentive On-Delay Timer Coil
- ---(SA) Off-Delay Timer Coil

13.2 Location of a Timer in Memory and Components of a Timer

Area in Memory

Timers have an area reserved for them in the memory of your CPU.

This memory area reserves one 16-bit word for each timer address.

The ladderlogic instruction set supports 256 timers.

Please refer to your CPU's technical information to establish the number of timer words available.

The following functions have access to the timer memory area:

- Timer instructions
- Updating of timer words by means of clock timing. This function of your CPU in the RUN mode decrements a given time value by one unit at the interval designated by the time base until the time value is equal to zero.

Time Value

Bits 0 through 9 of the timer word contain the time value in binary code.

The time value specifies a number of units.

Time updating decrements the time value by one unit at an interval designated by the time base.

Decrementing continues until the time value is equal to zero.

You can load a time value into the low word of accumulator 1 in binary, hexadecimal, or binary coded decimal (BCD) format.

You can pre-load a time value using either of the following formats:

- **W#16#wxyz**

- Where w = the time base (that is, the time interval or resolution)
- Where xyz = the time value in binary coded decimal format

- **S5T#aH_bM_cS_dMS**

- Where H = hours, M = minutes, S = seconds, and MS = milliseconds;
a, b, c, d are defined by the user.
- The time base is selected automatically, and the value is rounded to the next lower number with that time base.

The maximum time value that you can enter is 9,990 seconds, or
2H_46M_30S.

S5TIME#4S = 4 seconds s5t#2h_15m = 2 hours and 15 minutes

S5T#1H_12M_18S = 1 hour, 12 minutes, and 18 seconds

Time Base

Bits 12 and 13 of the timer word contain the time base in binary code.

The time base defines the interval at which the time value is decremented by one unit.

The smallest time base is 10 ms; the largest is 10 s.

Time Base	Binary Code for the Time Base
10 ms	00
100 ms	01
1 s	10
10 s	11

Values that exceed 2h46m30s are not accepted.

A value whose resolution is too high for the range limits (for example, 2h10ms) is truncated down to a valid resolution.

The general format for S5TIME has limits to range and resolution as shown below:

Resolution	Range
0.01 second	10MS to 9S_990MS
0.1 second	100MS to 1M_39S_900MS
1 second	1S to 16M_39S
10 seconds	10S to 2H_46M_30S

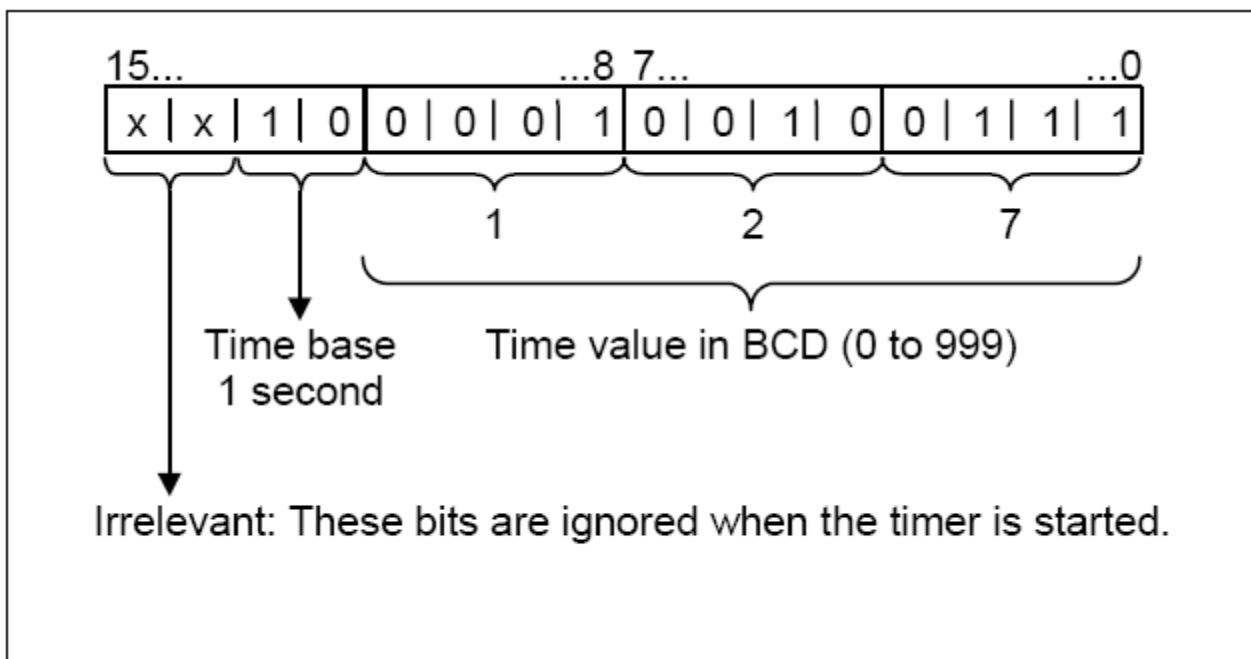
Bit Configuration in the Time Cell

When a timer is started, the contents of the timer cell are used as the time value.

Bits 0 through 11 of the timer cell hold the time value in binary coded decimal format (BCD format: each set of four bits contains the binary code for one decimal value).

Bits 12 and 13 hold the time base in binary code.

The following figure shows the contents of the timer cell loaded with timer value 127 and a time base of 1 second :



Reading the Time and the Time Base

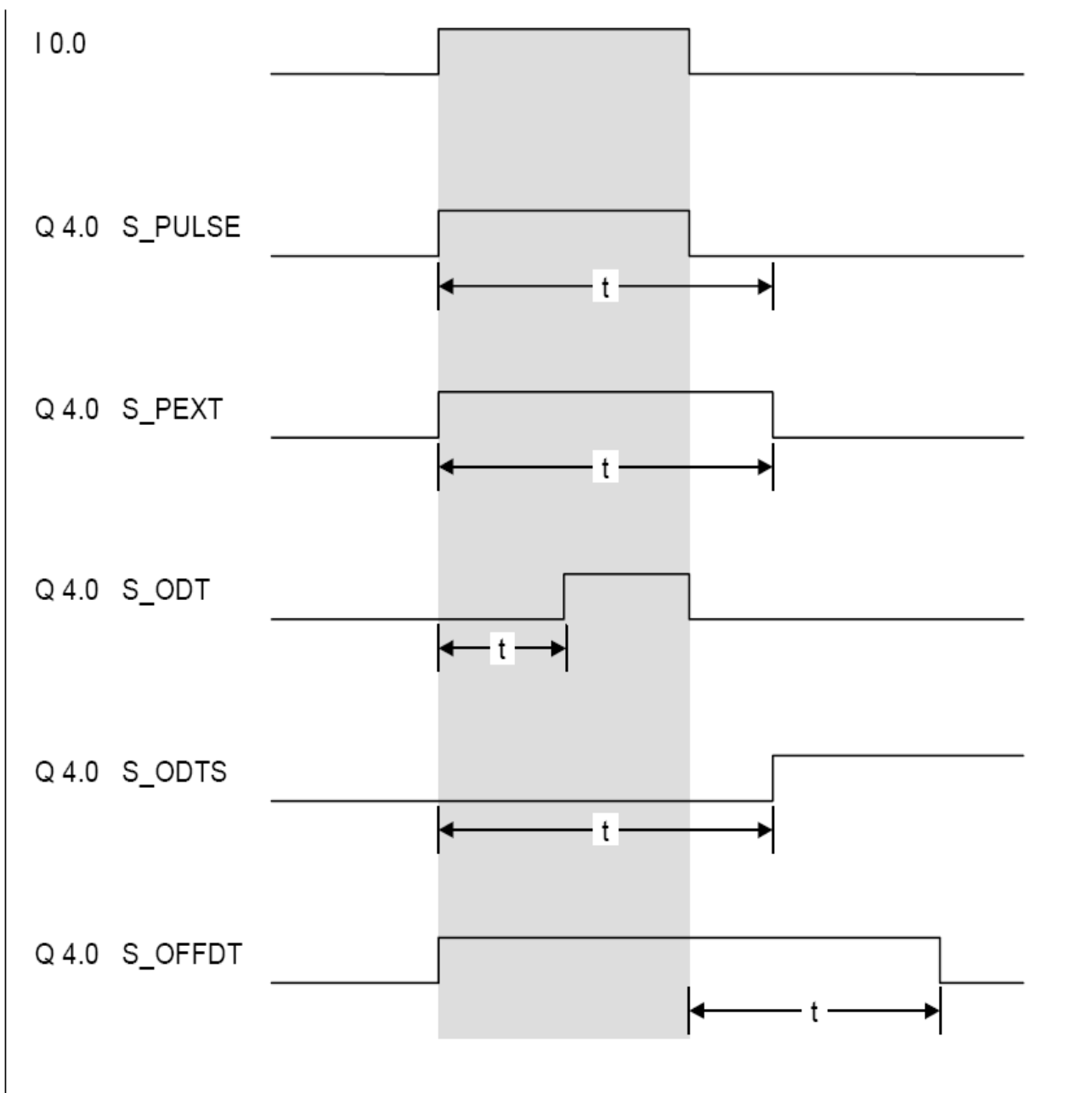
Each timer box provides two outputs, BI and BCD, for which you can indicate a word location.

The BI output provides the time value in binary format.

The BCD output provides the time base and the time value in binary coded decimal (BCD) format.

Choosing the right Timer

This overview is intended to help you choose the right timer for your timing job.

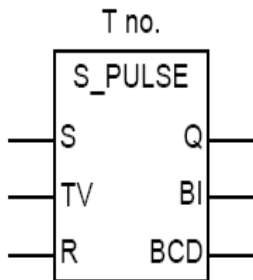


Timer	Description
S_PULSE Pulse timer	The maximum time that the output signal remains at 1 is the same as the programmed time value t . The output signal stays at 1 for a shorter period if the input signal changes to 0.
S_PEXT Extended pulse timer	The output signal remains at 1 for the programmed length of time, regardless of how long the input signal stays at 1.
S_ODT On-delay timer	The output signal changes to 1 only when the programmed time has elapsed and the input signal is still 1.
S_ODTS Retentive on-delay timer	The output signal changes from 0 to 1 only when the programmed time has elapsed, regardless of how long the input signal stays at 1.
S_OFFDT Off-delay timer	The output signal changes to 1 when the input signal changes to 1 or while the timer is running. The time is started when the input signal changes from 1 to 0.

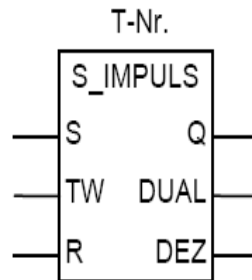
13.3 S_PULSE Pulse S5 Timer

Symbol

English



German



Parameter English	Parameter German	Data Type	Memory Area	Description
T no.	T-Nr.	TIMER	T	Timer identification number; range depends on CPU
S	S	BOOL	I, Q, M, L, D	Start input
TV	TW	S5TIME	I, Q, M, L, D	Preset time value
R	R	BOOL	I, Q, M, L, D	Reset input
BI	DUAL	WORD	I, Q, M, L, D	Remaining time value, integer format
BCD	DEZ	WORD	I, Q, M, L, D	Remaining time value, BCD format
Q	Q	BOOL	I, Q, M, L, D	Status of the timer

Description

S_PULSE (Pulse S5 Timer) starts the specified timer if there is a positive edge at the start (S) input.

A signal change is always necessary in order to enable a timer.

The timer runs as long as the signal state at input S is "1", the longest period,

however, is the time value specified by input TV.

The signal state at output Q is "1" as long as the timer is running.

If there is a change from "1" to "0" at the S input before the time interval has elapsed the timer will be stopped. In this case the signal state at output Q is "0".

The timer is reset when the timer reset (R) input changes from "0" to "1" while the timer is running.

The current time and the time base are also set to zero.

Logic "1" at the timer's R input has no effect if the timer is not running.

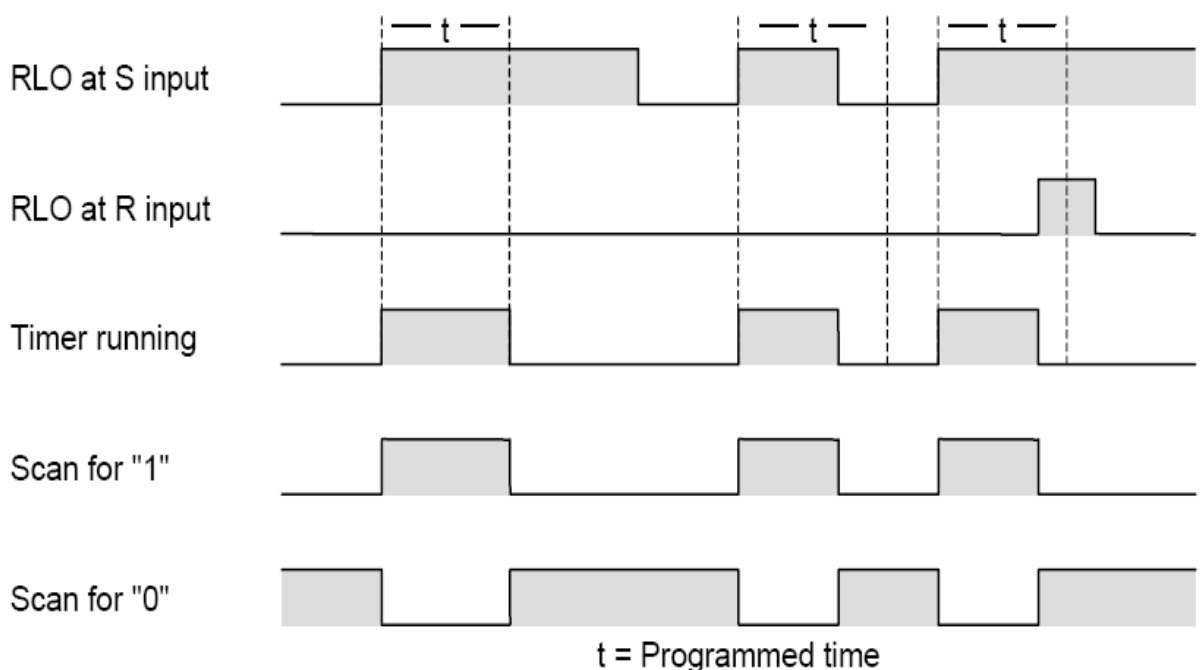
The current time value can be scanned at the outputs BI and BCD.

The time value at BI is binary coded, at BCD it is BCD coded.

The current time value is the initial TV value minus the time elapsed since the timer was started.

Timing Diagram

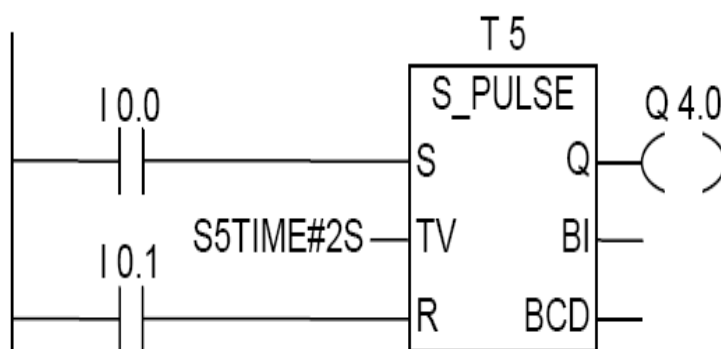
Pulse timer characteristics:



Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



If the signal state of input I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 will be started.

The timer will continue to run for the specified time of two seconds (2 s) as long as I0.0 is "1".

If the signal state of input I0.0 changes from "1" to "0" before the timer has expired the timer will be stopped.

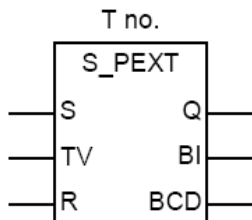
If the signal state of input I0.1 changes from "0" to "1" while the timer is running, the time is reset.

The output Q4.0 is logic "1" as long as the timer is running and "0" if the time has elapsed or was reset.

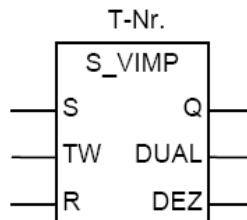
13.4 S_PEXT Extended Pulse S5 Timer

Symbol

English



German



Parameter English	Parameter German	Data Type	Memory Area	Description
T no.	T-Nr.	TIMER	T	Timer identification number; range depends on CPU
S	S	BOOL	I, Q, M, L, D	Start input
TV	TW	S5TIME	I, Q, M, L, D	Preset time value
R	R	BOOL	I, Q, M, L, D	Reset input
BI	DUAL	WORD	I, Q, M, L, D	Remaining time value, integer format
BCD	DEZ	WORD	I, Q, M, L, D	Remaining time value, BCD format
Q	Q	BOOL	I, Q, M, L, D	Status of the timer

Description

S_PEXT (Extended Pulse S5 Timer) starts the specified timer if there is a positive edge at the start (S) input.

A signal change is always necessary in order to enable a timer.

The timer runs for the preset time interval specified at input TV even if the signal state at the S input changes to "0" before the time interval has elapsed.

The signal state at output Q is "1" as long as the timer is running.

The timer will be restarted ("re-triggered") with the preset time value if the signal state at input S changes from "0" to "1" while the timer is running.

The timer is reset if the reset (R) input changes from "0" to "1" while the timer is running.

The current time and the time base are set to zero.

The current time value can be scanned at the outputs BI and BCD.

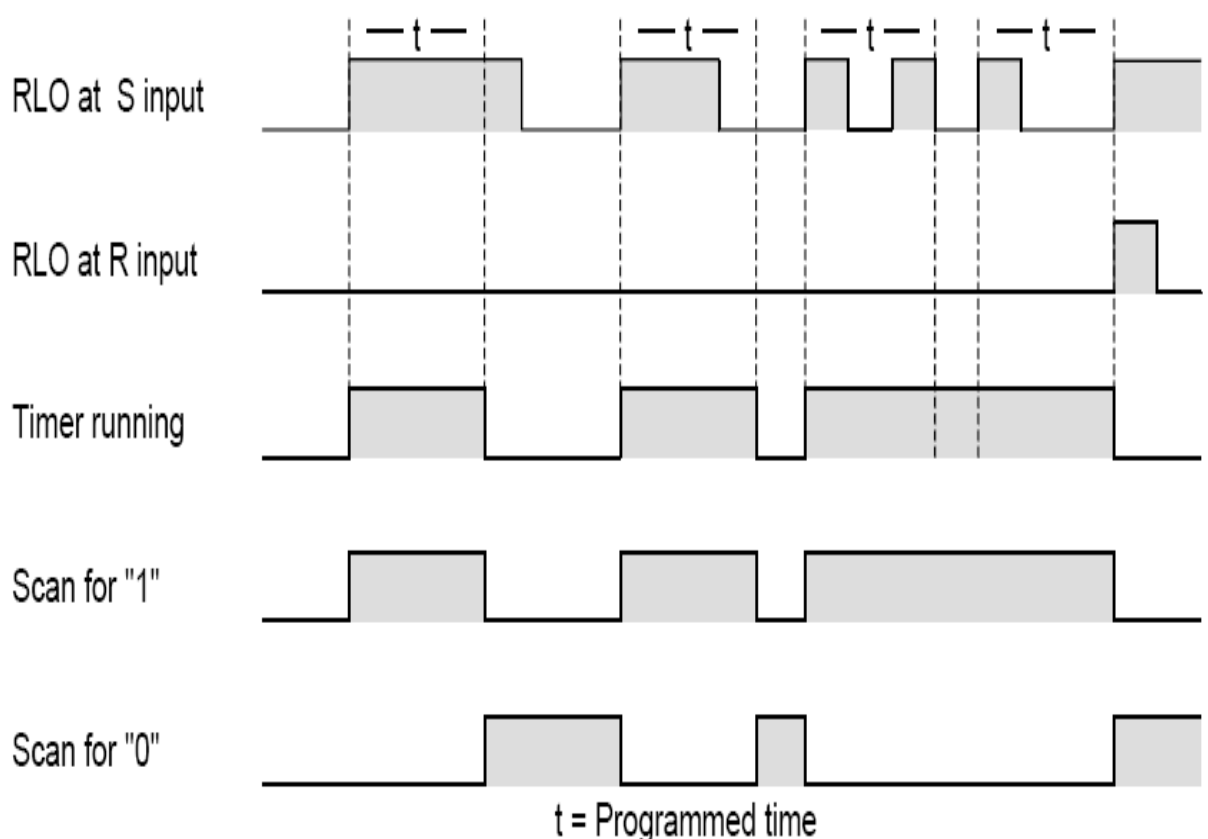
The time value at BI is binary coded, at BCD is BCD coded.

The current time value is the initial TV value minus the time elapsed since the timer was started.

See also "Location of a Timer in Memory and Components of a Timer".

Timing Diagram

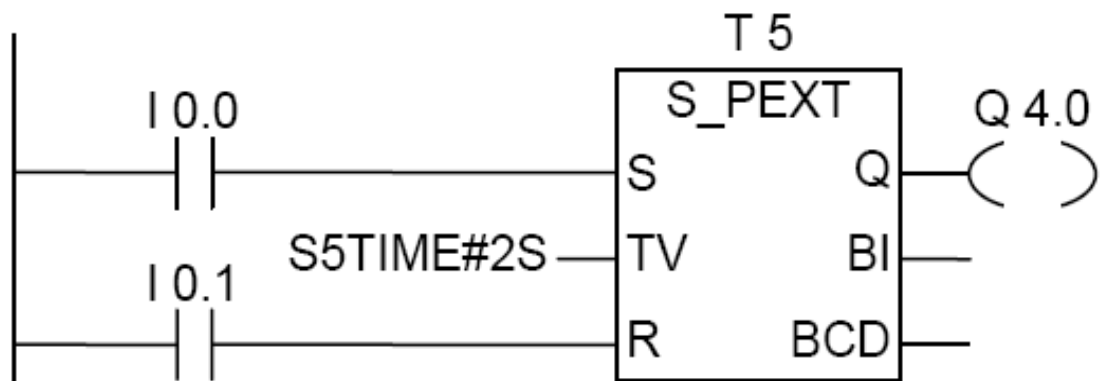
Extended pulse timer characteristics:



Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	X	X	X	1

Example



If the signal state of input I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 will be started.

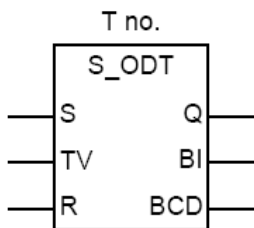
The timer will continue to run for the specified time of two seconds (2 s) without being affected by a negative edge at input S.

If the signal state of I0.0 changes from "0" to "1" before the timer has expired the timer will be re-triggered. The output Q4.0 is logic "1" as long as the timer is running.

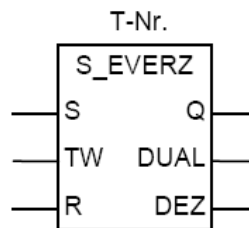
13.5 S_ODT On-Delay S5 Timer

Symbol

English



German



Parameter English	Parameter German	Data Type	Memory Area	Description
T no.	T-Nr.	TIMER	T	Timer identification number; range depends on CPU
S	S	BOOL	I, Q, M, L, D	Start input
TV	TW	S5TIME	I, Q, M, L, D	Preset time value
R	R	BOOL	I, Q, M, L, D	Reset input
BI	DUAL	WORD	I, Q, M, L, D	Remaining time value, integer format
BCD	DEZ	WORD	I, Q, M, L, D	Remaining time value, BCD format
Q	Q	BOOL	I, Q, M, L, D	Status of the timer

Description

S_ODT (On-Delay S5 Timer) starts the specified timer if there is a positive edge at the start (S) input.

A signal change is always necessary in order to enable a timer.

The timer runs for the time interval specified at input TV as long as the signal state at input S is positive.

The signal state at output Q is "1" when the timer has elapsed without

error and the signal state at the S input is still "1".

When the signal state at input S changes from "1" to "0" while the timer is running, the timer is stopped.

In this case the signal state of output Q is "0".

The timer is reset if the reset (R) input changes from "0" to "1" while the timer is running. The current time and the time base are set to zero.

The signal state at output Q is then "0".

The timer is also reset if there is a logic "1" at the R input while the timer is not running and the RLO at input S is "1".

The current time value can be scanned at the outputs BI and BCD.

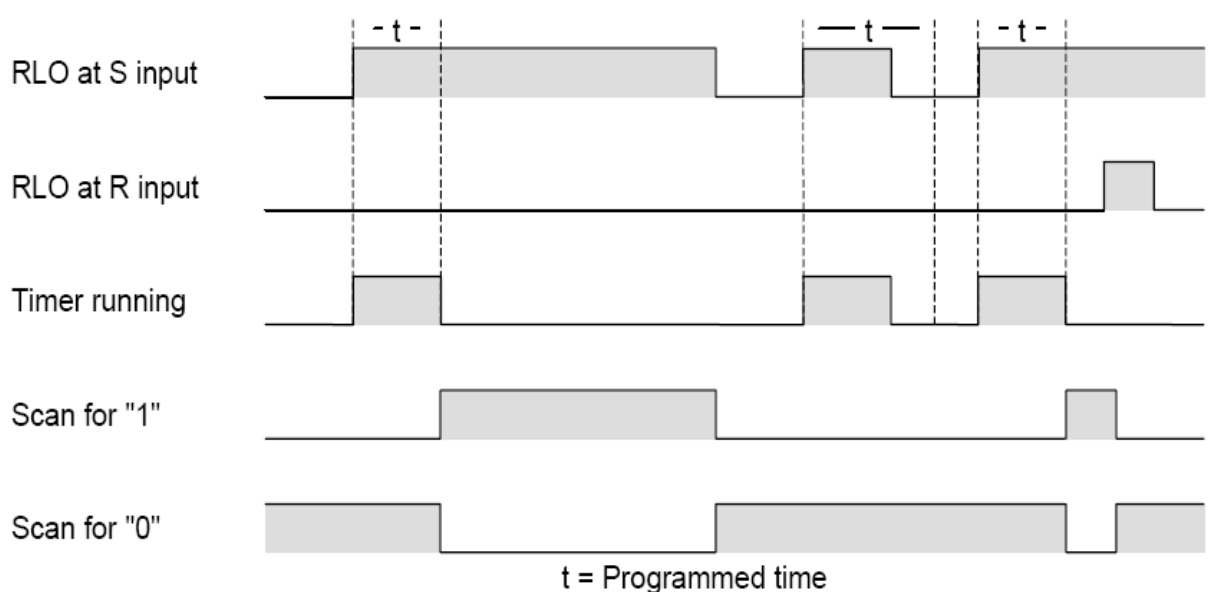
The time value at BI is binary coded, at BCD is BCD coded.

The current time value is the initial TV value minus the time elapsed since the timer was started.

See also "Location of a Timer in Memory and Components of a Timer".

Timing Diagram

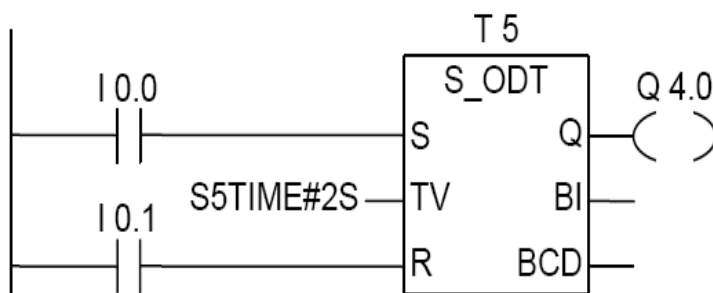
On-Delay timer characteristics:



Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	x	x	x	1

Example



If the signal state of I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 will be started. If the time of two seconds elapses and the signal state at input I0.0 is still "1", the output Q4.0 will be "1".

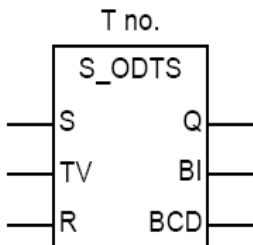
If the signal state of I0.0 changes from

"1" to "0", the timer is stopped and Q4.0 will be "0" (if the signal state of I0.1 changes from "0" to "1", the time is reset regardless of whether the timer is running or not).

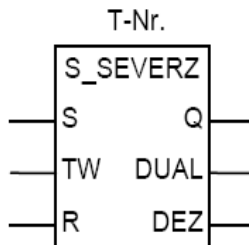
13.6 S_ODTS Retentive On-Delay S5 Timer

Symbol

English



German



Parameter English	Parameter German	Data Type	Memory Area	Description
T no.	T-Nr.	TIMER	T	Timer identification number; range depends on CPU
S	S	BOOL	I, Q, M, L, D	Start input
TV	TW	S5TIME	I, Q, M, L, D	Preset time value
R	R	BOOL	I, Q, M, L, D	Reset input
BI	DUAL	WORD	I, Q, M, L, D	Remaining time value, integer format
BCD	DEZ	WORD	I, Q, M, L, D	Remaining time value, BCD format
Q	Q	BOOL	I, Q, M, L, D	Status of the timer

Description

S_ODTS (Retentive On-Delay S5 Timer) starts the specified timer if there is a positive edge at the start (S) input.

A signal change is always necessary in order to enable a timer.

The timer runs for the time interval specified at input TV even if the signal state at input S changes to "0" before the time interval has elapsed.

The signal state at output Q is "1" when the timer has elapsed without

regard to the signal state at input S.

The timer will be restarted (re-triggered) with the specified time if the signal state at input S changes from "0" to "1" while the timer is running.

The timer is reset if the reset (R) input changes from "0" to "1" without regard to the RLO at the S input. The signal state at output Q is then "0".

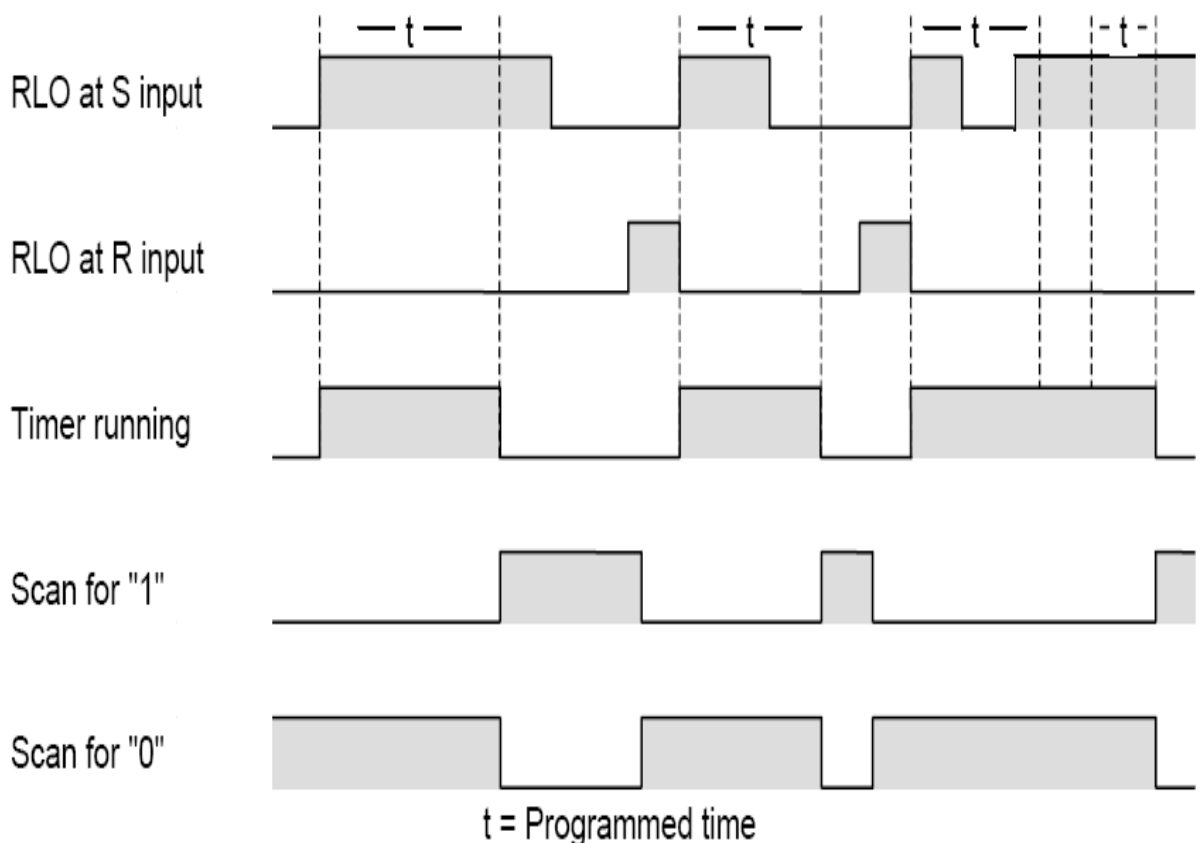
The current time value can be scanned at the outputs BI and BCD.

The time value at BI is binary coded, at BCD it is BCD coded.

The current time value is the initial TV value minus the time elapsed since the timer was started.

Timing Diagram

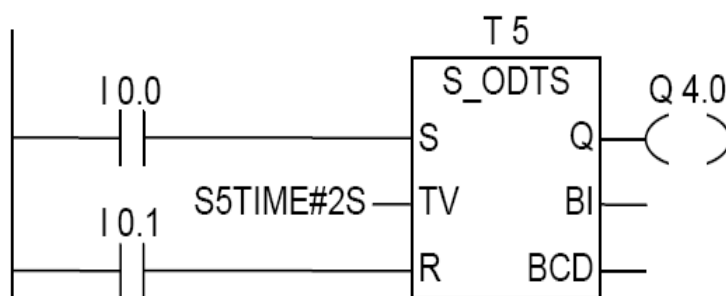
Retentive On-Delay timer characteristics:



Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	x	x	x	1

Example



If the signal state of I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 will be started.

The timer runs without regard to a signal change at I0.0 from "1" to "0".

If the signal state at I0.0 changes from "0" to "1" before the timer has expired, the timer will be re-triggered.

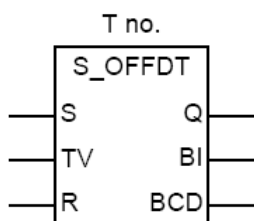
The output Q4.0 will be "1" if the timer elapsed.

(If the signal state of input I0.1 changes from "0" to "1", the time will be reset irrespective of the RLO at S.)

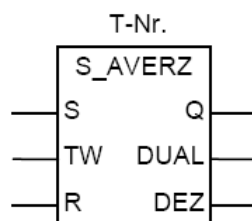
13.7 S_OFFDT Off-Delay S5 Timer

Symbol

English



German



Parameter English	Parameter German	Data Type	Memory Area	Description
T no.	T-Nr.	TIMER	T	Timer identification number; range depends on CPU
S	S	BOOL	I, Q, M, L, D	Start input
TV	TW	S5TIME	I, Q, M, L, D	Preset time value
R	R	BOOL	I, Q, M, L, D	Reset input
BI	DUAL	WORD	I, Q, M, L, D	Remaining time value, integer format
BCD	DEZ	WORD	I, Q, M, L, D	Remaining time value, BCD format
Q	Q	BOOL	I, Q, M, L, D	Status of the timer

Description

S_OFFDT (Off-Delay S5 Timer) starts the specified timer if there is a negative edge at the start (S) input. A signal change is always necessary in order to enable a timer.

The signal state at output Q is "1" if the signal state at the S input is "1" or while the timer is running.

The timer is reset when the signal state at input S goes from "0" to "1" while the timer is running. The timer is not restarted until the signal state at input S changes again from "1" to "0".

The timer is reset when the reset (R) input changes from "0" to "1" while the timer is running.

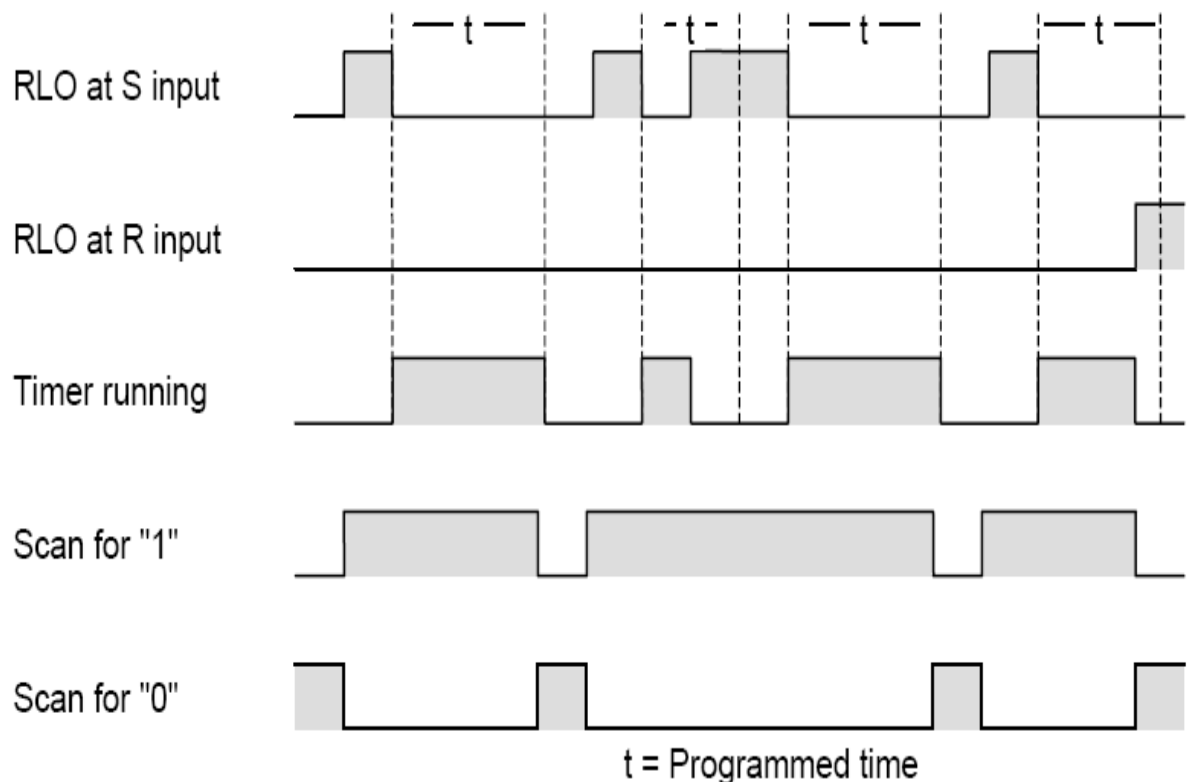
The current time value can be scanned at the outputs BI and BCD.

The time value at BI is binary coded, at BCD it is BCD coded.

The current time value is the initial TV value minus the time elapsed since the timer was started.

Timing Diagram

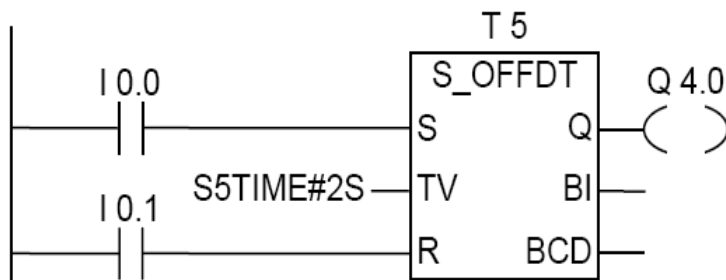
Off-Delay timer characteristics:



Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	x	x	x	1

Example



If the signal state of I0.0 changes from "1" to "0", the timer is started.

Q4.0 is "1" when I0.0 is "1" or the timer is running. (if the signal state at I0.1 changes from "0" to "1" while the time is running, the timer is reset).

13.8 ---(SP) Pulse Timer Coil

Symbol

English	German
<T no..>	<T no.>
---(SP)	---(SI)
<time value>	<time value>

Parameter	Data Type	Memory Area	Description
<T no.>	TIMER	T	Timer identification number; range depends on CPU
<time value>	S5TIME	I, Q, M, L, D	Preset time value

Description

---(SP) (Pulse Timer Coil) starts the specified timer with the **<time value>** when there is a positive edge on the RLO state.

The timer continues to run for the specified time interval as long as the RLO remains positive ("1").

The signal state of the counter is "1" as long as the timer is running.

If there is a change from "1" to "0" in the RLO before the time value has elapsed, the timer will stop.

In this case, a scan for "1" always produces the result "0".

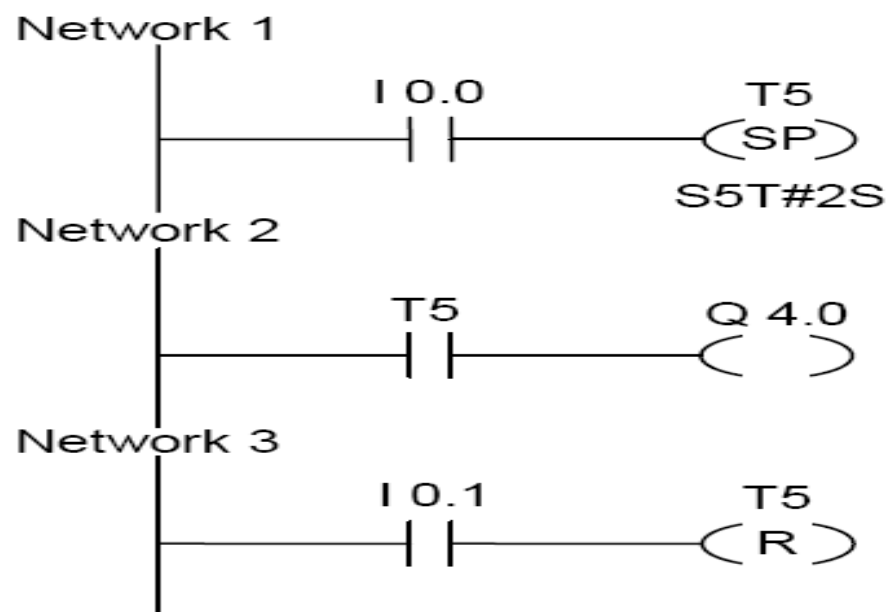
See also "Location of a Timer in Memory and Components of a Timer" and

S_PULSE (Pulse S5 Timer).

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	-	-	0

Example



If the signal state of input I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 is started.

The timer continues to run with the specified time of two seconds as long as the signal state of input I0.0 is "1".

If the signal state of input I0.0 changes from "1" to "0" before the specified time has elapsed, the timer stops.

The signal state of output Q4.0 is "1" as long as the timer is running.

A signal state change from "0" to "1" at input I0.1 will reset timer T5 which stops the timer and clears the remaining portion of the time value to "0".

13.9 ---(SE) Extended Pulse Timer Coil

Symbol

English	German
<T no.>	<T no>
---(SE)	---(SV)
<time value>	<time value>

Parameter	Data Type	Memory Area	Description
<T no.>	TIMER	T	Timer identification number; range depends on CPU
<time value>	S5TIME	I, Q, M, L, D	Preset time value

Description

---(SE) (Extended Pulse Timer Coil) starts the specified timer with the specified **<time value>** when there is a positive edge on the RLO state.

The timer continues to run for the specified time interval even if the RLO changes to "0" before the timer has expired.

The signal state of the counter is "1" as long as the timer is running.

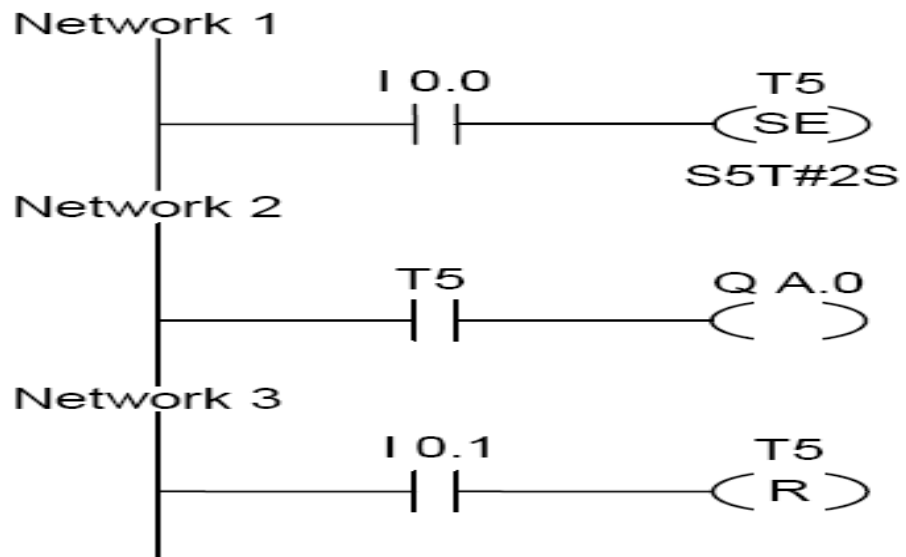
The timer will be restarted (re-triggered) with the specified time value if the RLO changes from "0" to "1" while the timer is running.

See also "Location of a Timer in Memory and Components of a Timer" and S_PEXT (Extended Pulse S5 Timer).

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	-	-	0

Example



If the signal state of input I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 is started.

The timer continues to run without regard to a negative edge of the RLO.

If the signal state of I0.0 changes from "0" to "1" before the timer has expired, the timer is re-triggered.

The signal state of output Q4.0 is "1" as long as the timer is running.

A signal state change from "0" to "1" at input I0.1 will reset

timer T5 which stops the timer and clears the remaining portion of the time value to "0".

13.10 ---(SD) On-Delay Timer Coil

Symbol

English	German
<T no.>	<T no.>
---(SD)	---(SE)
<time value>	<time value>

Parameter	Data Type	Memory Area	Description
<T no.>	TIMER	T	Timer identification number; range depends on CPU
<time value>	S5TIME	I, Q, M, L, D	Preset time value

Description

---(SD) (On Delay Timer Coil) starts the specified timer with the **<time value>** if there is a positive edge on the RLO state.

The signal state of the timer is "1" when the **<time value>** has elapsed without error and the RLO is still "1".

When the RLO changes from "1" to "0" while the timer is running, the timer is reset.

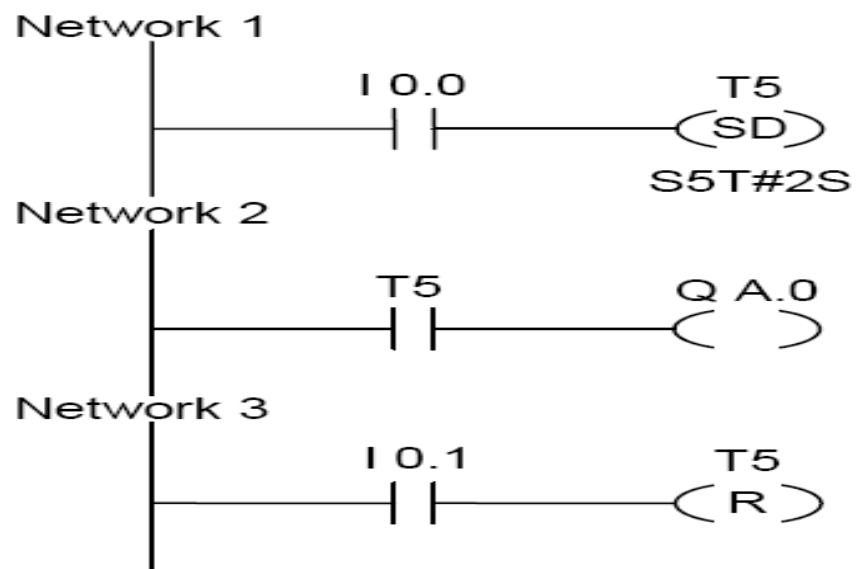
In this case, a scan for "1" always produces the result "0".

See also "Location of a Timer in Memory and Components of a Timer" and S_ODT (On-Delay S5 Timer).

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	-	-	0

Example



If the signal state of input I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 is started.

If the time elapses and the signal state of input I0.0 is still "1", the signal state of output Q4.0 will be "1".

If the signal state of input I0.0 changes from "1" to "0", the timer remains idle and the signal state of output Q4.0 will be "0".

A signal state change from "0" to "1" at input I0.1 will reset timer T5 which stops the timer and clears the remaining portion of the time value to "0".

13.11 ---(SS) Retentive On-Delay Timer Coil

Symbol

English	German
<T no.>	<T no.>
---(SS)	---(SS)
<time value>	<time value>

Parameter	Data Type	Memory Area	Description
<T no.>	TIMER	T	Timer identification number; range depends on CPU
<time value>	S5TIME	I, Q, M, L, D	Preset time value

Description

---(SS) (Retentive On-Delay Timer Coil) starts the specified timer if there is a positive edge on the RLO state.

The signal state of the timer is "1" if the time value has elapsed.

A restart of the timer is only possible if it is reset explicitly.

Only a reset causes the signal state of the timer to be set to "0".

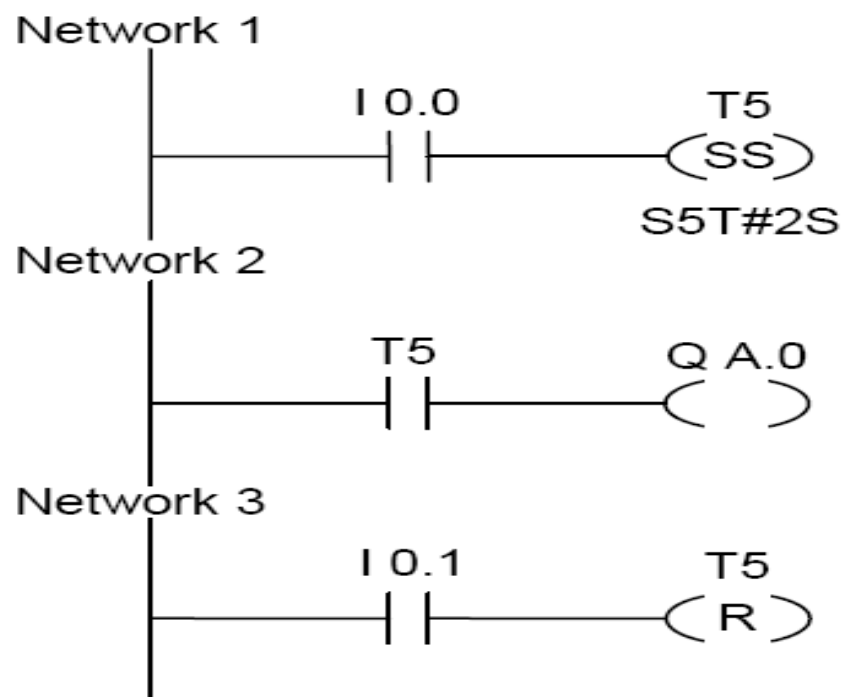
The timer restarts with the specified time value if the RLO changes from "0" to "1" while the timer is running.

See also "Location of a Timer in Memory and Components of a Timer" and S_ODTS (Retentive On-Delay S5 Timer).

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	-	-	0

Example



If the signal state of input I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 is started.

If the signal state of input I0.0 changes from "0" to "1" before the timer has expired, the timer is re-triggered.

The output Q4.0 will be "1" if the timer elapsed.

A signal state "1" at input I0.1 will reset timer T5, which stops the timer and clears the remaining portion of the time value to "0".

13.12 ---(SF) Off-Delay Timer Coil

Symbol

English	German
<T no.>	<T no.>
---(SF)	---(SA)
<time value>	<time value>

Parameter	Data Type	Memory Area	Description
<T no.>	TIMER	T	Timer identification number; range depends on CPU
<time value>	S5TIME	I, Q, M, L, D	Preset time value

Description

---(SF) (Off-Delay Timer Coil) starts the specified timer if there is a negative edge on the RLO state.

The timer is "1" when the RLO is "1" or as long as the timer is running during the **<time value>** interval.

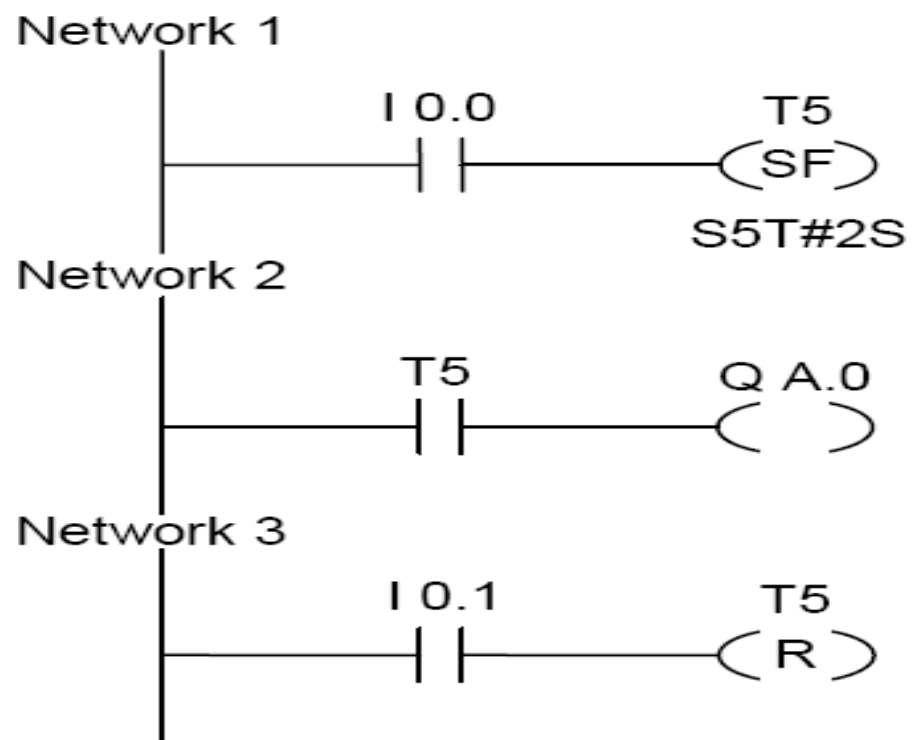
The timer is reset when the RLO goes from "0" to "1" while the timer is running. The timer is always restarted when the RLO changes from "1" to "0".

See also "Location of a Timer in Memory and Components of a Timer" and S_OFFDT (Off-Delay S5 Timer).

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	-	-	-	-	-	0	-	-	0

Example



If the signal state of input I0.0 changes from "1" to "0" the timer is started. The signal state of output Q4.0 is "1" when input I0.0 is "1" or the timer is running.

A signal state change from "0" to "1" at input I0.1 will reset timer T5 which stops the timer and clears the remaining portion of the time value to "0".

14 Word Logic Instructions

14.1 Overview of Word logic instructions

Description

Word logic instructions compare pairs of words (16 bits) and double words (32 bits) bit by bit, according to Boolean logic.

If the result at output OUT does not equal 0, bit CC 1 of the status word is set to "1".

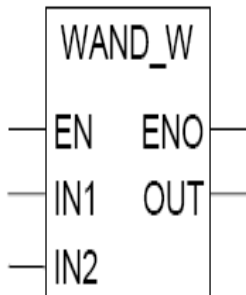
If the result at output OUT does equal 0, bit CC 1 of the status word is set to "0".

The following word logic instructions are available:

- **WAND_W** (Word) AND Word
- **WOR_W** (Word) OR Word
- **WXOR_W** (Word) Exclusive OR Word
- **WAND_DW** (Word) AND Double Word
- **WOR_DW** (Word) OR Double Word
- **WXOR_DW** (Word) Exclusive OR Double Word

14.2 WAND_W (Word) AND Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	WORD	I, Q, M, L, D	First value for logic operation
IN2	WORD	I, Q, M, L, D	Second value for logic operation
OUT	WORD	I, Q, M, L, D	Result word of logic operation

Description

WAND_W (AND Words) is activated by signal state "1" at the enable (EN) input and Ands the two word values present at IN1 and IN2 bit by bit.

The values are interpreted as pure bit patterns.

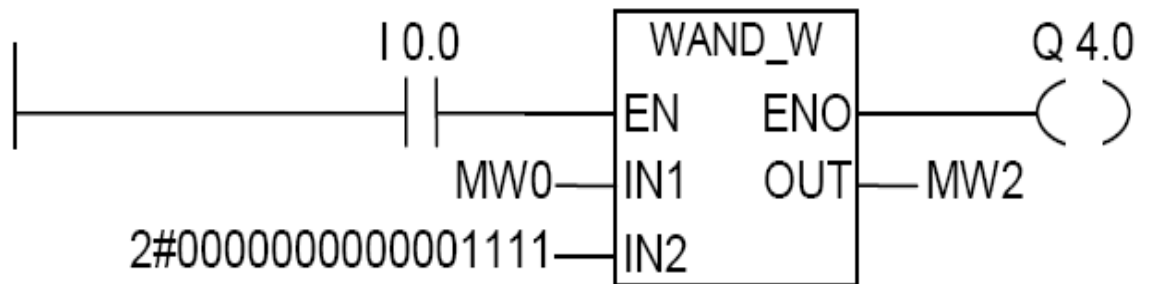
The result can be scanned at the output OUT.

ENO has the same logic state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	x	0	0	-	x	1	1	1

Example



The instruction is executed if I0.0 is "1".

Only bits 0 to 3 of MW0 are relevant, the rest of MW0 is masked by the IN2

word bit pattern:

MW0 = 01010101 01010101

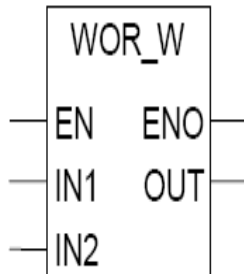
IN2 = 00000000 00001111

MW0 AND IN2 = MW2 = 00000000 00000101

Q4.0 is "1" if the instruction is executed.

14.3 WOR_W (Word) OR Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	WORD	I, Q, M, L, D	First value for logic operation
IN2	WORD	I, Q, M, L, D	Second value for logic operation
OUT	WORD	I, Q, M, L, D	Result word of logic operation

Description

WOR_W (OR Words) is activated by signal state "1" at the enable (EN) input and ORs the two word values present at IN1 and IN2 bit by bit. The values are interpreted as pure bit patterns.

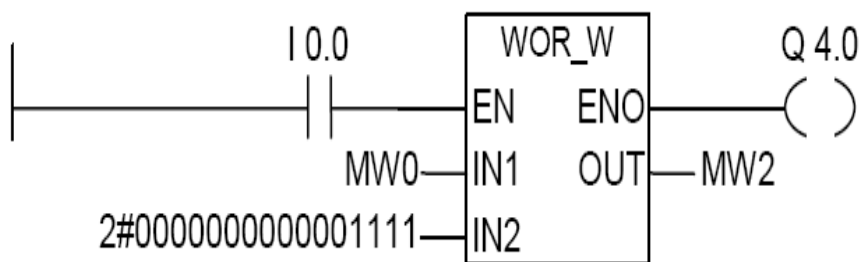
The result can be scanned at the output OUT.

ENO has the same logic state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	x	0	0	-	x	1	1	1

Example



The instruction is executed if I0.0 is "1".

Bits 0 to 3 are set to "1", all other MW0 bits are not changed.

MW0 = 01010101 01010101

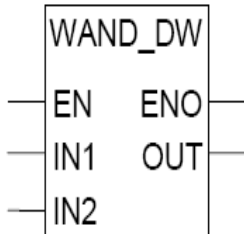
IN2 = 00000000 00001111

MW0 OR IN2 = MW2 = 01010101 01011111

Q4.0 is "1" if the instruction is executed.

14.4 WAND_DW (Word) AND Double Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	DWORD	I, Q, M, L, D	First value for logic operation
IN2	DWORD	I, Q, M, L, D	Second value for logic operation
OUT	DWORD	I, Q, M, L, D	Result double word of logic operation

Description

WAND_DW (AND Double Words) is activated by signal state "1" at the enable (EN) input and ANDs the two word values present at IN1 and IN2 bit by bit.

The values are interpreted as pure bit patterns.

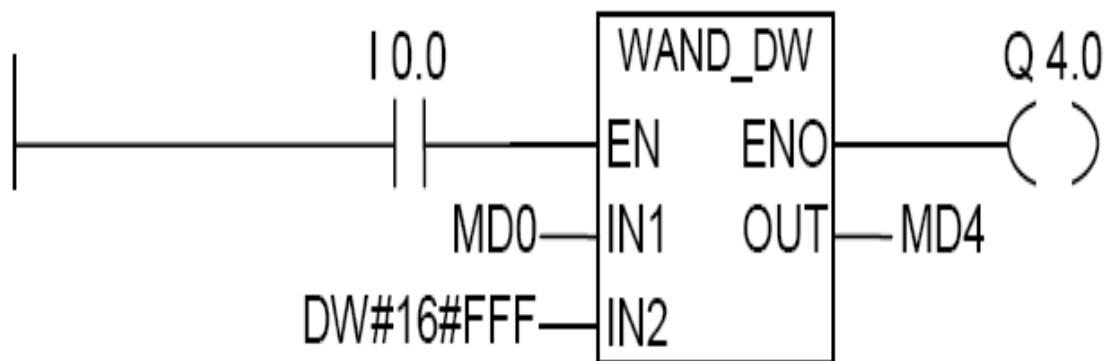
The result can be scanned at the output OUT.

ENO has the same logic state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	x	0	0	-	x	1	1	1

Example



The instruction is executed if I0.0 is "1".

Only bits 0 and 11 of MD0 are relevant, the rest of MD0 is masked by the IN2 bit pattern:

MD0 = 01010101 01010101 01010101 01010101

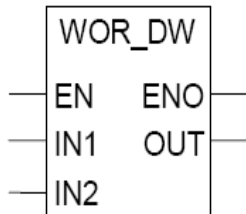
IN2 = 00000000 00000000 00001111 11111111

MD0 AND IN2 = MD4 = 00000000 00000000 00000101
01010101

Q4.0 is "1" if the instruction is executed.

14.5 WOR_DW (Word) OR Double Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	DWORD	I, Q, M, L, D	First value for logic operation
IN2	DWORD	I, Q, M, L, D	Second value for logic operation
OUT	DWORD	I, Q, M, L, D	Result double word of logic operation

Description

WOR_DW (OR Double Words) is activated by signal state "1" at the enable (EN) input and ORs the two word values present at IN1 and IN2 bit by bit.

The values are interpreted as pure bit patterns.

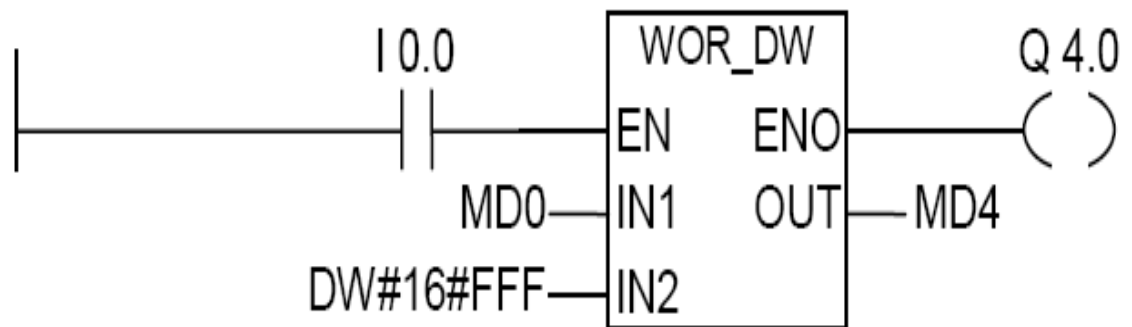
The result can be scanned at the output OUT.

ENO has the same logic state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	x	0	0	-	x	1	1	1

Example



The instruction is executed if I0.0 is "1".

Bits 0 to 11 are set to "1", the remaining MD0 bits are not changed:

MD0 = 01010101 01010101 01010101 01010101

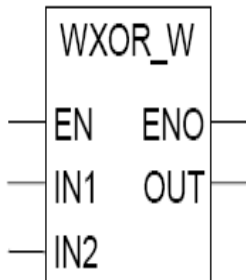
IN2 = 00000000 00000000 00001111 11111111

MD0 OR IN2 = MD4 = 01010101 01010101 01011111 11111111

Q4.0 is "1" if the instruction is executed.

14.6 WXOR_W (Word) Exclusive OR Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	WORD	I, Q, M, L, D	First value for logic operation
IN2	WORD	I, Q, M, L, D	Second value for logic operation
OUT	WORD	I, Q, M, L, D	Result word of logic operation

Description

WXOR_W (Exclusive OR Word) is activated by signal state "1" at the enable (EN) input and XORs the two word values present at IN1 and IN2 bit by bit.

The values are interpreted as pure bit patterns.

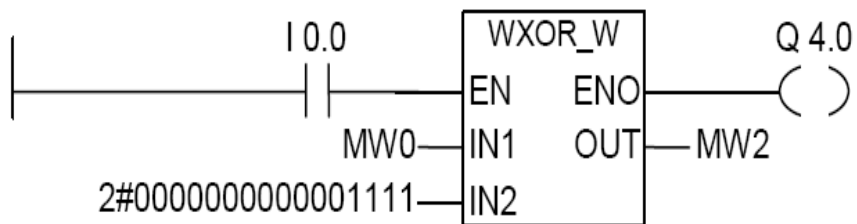
The result can be scanned at the output OUT.

ENO has the same logic state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	x	0	0	-	x	1	1	1

Example



The instruction is executed if I0.0 is "1":

MW0 = 01010101 01010101

IN2 = 00000000 00001111

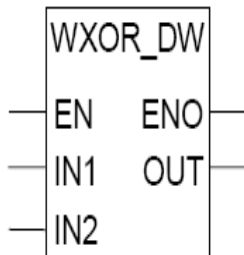
MW0 XOR IN2 = MW2 = 01010101 01011010

Q4.0 is "1" if the instruction is executed.

14.7 WXOR_DW (Word) Exclusive OR

Double Word

Symbol



Parameter	Data Type	Memory Area	Description
EN	BOOL	I, Q, M, L, D	Enable input
ENO	BOOL	I, Q, M, L, D	Enable output
IN1	DWORD	I, Q, M, L, D	First value for logic operation
IN2	DWORD	I, Q, M, L, D	Second value for logic operation
OUT	DWORD	I, Q, M, L, D	Result double word of logic operation

Description

WXOR_DW (Exclusive OR Double Word) is activated by signal state "1" at the enable (EN) input and XORs the two word values present at IN1 and IN2 bit by bit.

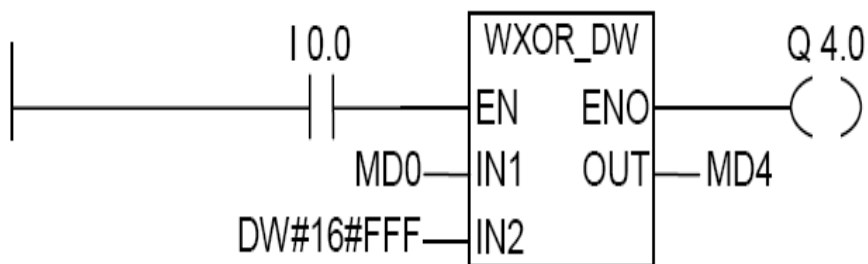
The values are interpreted as pure bit patterns. The result can be scanned at the output OUT.

ENO has the same logic state as EN.

Status word

	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
writes:	1	x	0	0	-	x	1	1	1

Example



The instruction is executed if I0.0 is "1":

MD0 = 01010101 01010101 01010101 01010101

IN2 = 00000000 00000000 00001111 11111111

MW2 = MD0 XOR IN2 = 01010101 01010101 01011010 10101010

Q4.0 is "1" if the instruction is executed.

